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Engineering Description of the ElectroData* Digital Computer

J. C. ALRICH†

Summary—The operation of the ElectroData digital computer, ntrol console, input-output equipment, and power units is de-ribed. The chief logical components are described in detail and the aracteristics of some circuits are given, with a description of logical eration. Basic design decisions are stated.

General Description

THE ELECTRODATA system to be described is composed of an electronic digital computer, a control console, a typewriter control unit, a punched rd converter unit, and a power control unit. Each of ese sections occupies a separate housing to permit rangements depending on the needs of each installa-on. Magnetic tape auxiliary storage units, with a pacity of 160,000 words each, are available to operate

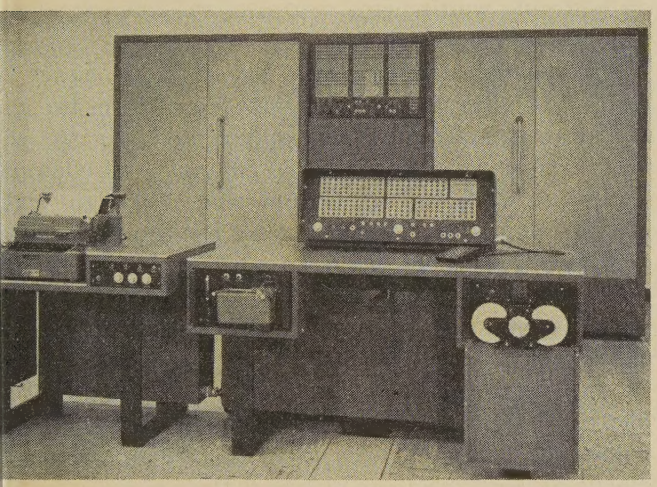

Fig. 1—ElectroData computer, console, and typewriter control.

th the system described here. Fig. 1 is a photograph the computer, the console, and the typewriter control.

gital Computer

The computer is an internally programmed magnetic um machine with single address fixed decimal point eration. Numbers are represented as absolute value d sign. The decimal point is at the left, and digits are presented in 1-2-4-8 binary code. Word length is 10 gits and sign; plus and minus are represented by the nventional 0 and 1, respectively, and appear at the t of the number. Throughout the system, decimal gits are transferred serially, bits of a digit are trans-red in parallel.

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The magnetic drum stores 4,000 words with a mean random access time of 8.5 milliseconds and 80 words in four 20-word quick-access sections with a mean random access time of 0.85 millisecond. Commands which facilitate use of the quick-access loops in a program effectively increase the drum speed from 3,550 rpm to about 25,000 rpm. A band-switching time less than 5 microseconds permits uninterrupted operation across bands. A nonreturn-to-zero recording system is used.

All arithmetic and logical operations are realized as static dc levels generated by flip-flops, and information is transferred or converted by means of pulses. The contents of all registers and the states of logical flip-flops are shown in neon lights on a supervisory control panel in the upper center section of the computer cabinet, shown in Fig. 2. Any flip-flop can be set to "one" or "zero" by depressing a push button associated with it.

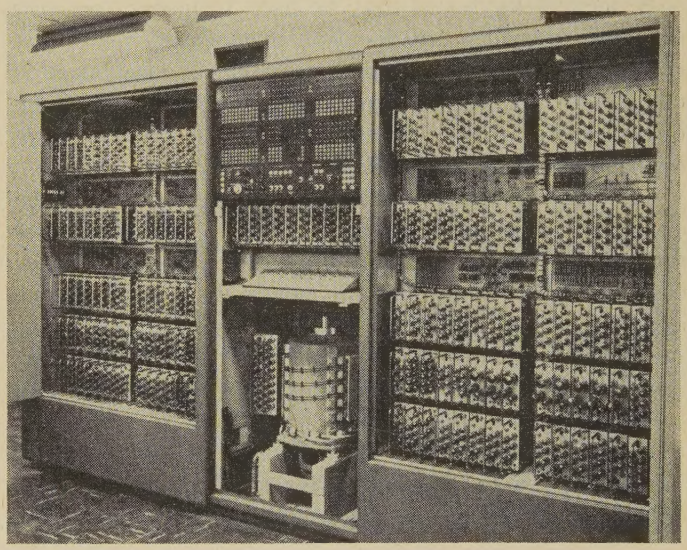


Fig. 2—ElectroData computer in open position.

The computer has a vocabulary of 55 orders, but as many as 100 might be wired into the control section with the present logic. A command word contains a two-digit order and a four-digit address, the order occupying the fifth and sixth digit positions and the address the last four digit positions of the word. The first four digits and the sign digit of a command are reserved as special programming aids.

Control Console

The console provides controls and remote indicators required for operating the system. These include neon lights for all the registers; a breakpoint switch to stop

the computation after the execution of commands containing coded breakpoint digits; and switches and push buttons to start and stop computation or input-output equipment.

The photoelectric tape reader is in the console, to the right of the operator (see Fig. 1). The reader reads punched paper tape into the computer at a rate of 540 characters per second, or 45 full computer words consisting of 10 digits, sign, and finish pulse. The tape uses a 6-hole code with digits represented in binary-coded decimal form. The fifth hole acts as a clock and distinguishes zero from blank tape. The sixth hole is present to generate a finish pulse at the end of a word.

The starting of the tape reader is under control of the computer. After the desired information has been read, a tape control instruction on the tape returns control to the computer. Variations of the instruction permit stopping the reader or allowing it to continue running, in cases where computations are short enough to be completed before the next word is sent into the machine.

A tape magazine attachment holds enough tape to store 4,000 words. A loop-adapter attachment permits the use of continuous loops or loose lengths of tape too short to warrant use of the magazine.

A decimal keyboard may be used to insert operands or commands into any location in storage or to insert commands into the command register. The keyboard is convenient for setting up simple programs to check operations or to call out words from selected storage locations into the accumulator, or A-register.

The tape punch is in the console, to the left of the operator. It punches paper tape at 13 characters per second. The starting and stopping of the punch is under control of the computer. All words are read from the accumulator. Output is numeric or alphanumeric. Numeric output is compatible with the input requirements, and output tapes can be read into the computer with no conversion. For alphanumeric print-out, an octal code is used. Each pair of octal numbers is translated, on instruction, into an alphanumeric character by the translator section in the typewriter control.

Typewriter Control

The typewriter control unit consists of an electric typewriter with mechanical tape punch and reader, a format control, a sign translator, a zero-suppress switch, and an alphanumeric translator (see Fig. 1). The typewriter operates at a rate of 10 characters per second, including alphanumeric print-out.

The format is controlled by either the format control or stored instructions within the computer or by both. The format control can be used to set the number of words per line, lines per group, and groups per page, actuating space or tab between words, carriage return at the end of line, and stopping the typewriter as necessary, with no internal programming. The sign translator converts the sign digit of each word received from the computer into the corresponding typewriter codes for plus and minus signs. The operator has the option, by closing a switch on the format control panel, of suppressing zeros to the left of the most significant digit of each word as it is typed out. The basic principle of the operation of the alphanumeric translator has been touched on in the section describing the tape punch. The typewriter can operate directly upon information received from the accumulator and alphanumeric translator and print out a completely general format limited only by the fact that paper feed in the typewriter goes in only one direction.

Punched Card Converter

The punched card converter is used to link an IBM summary punch to transfer data into the computer or to punch data into cards from the computer. It may also be used to operate a multibar tabulator. From 1 to 8 words per card, as selected by a rotary switch on the converter, can be read in at the rate of the punch, usually 100 cards per minute. As many as 1,000 cards may be read on a single command with the first word being read into the location shown by the command and all following words being read into the following memory locations in sequence.

Holes punched in the digit rows passing under the reading brushes permit the timed pulses from the card reader to energize 80 corresponding relays in the converter. Since the cards have 80 columns and computer words are each ten digits and sign, the eight extra spaces required to hold the sign for 8-word-per-card operation are made by overpunching in the X-row. After the reading brushes have energized corresponding relays among the 88 in the converter, the closed contacts are scanned with a diode matrix. A counter impulsed by the timed digits in the IBM unit translates the mercury-relay closure to the proper binary-coded digit value. This digit value is then inserted in the proper digit and word positions of one of the quick-access sections on the drum. This process continues until the sign and digit values from 9 through 0 have been read into storage from the card.

When all the words have been read from a card, an automatic block transfer is initiated to transfer information from the quick-access section to a selected series of addresses in main memory. This operation is repeated until all cards have been read, the number of which was indicated in the instruction. Otherwise, the computer idles during this cycle.

Output operation of the converter is the reverse of the input operation just described. The number of words per card or per line, up to 8, is selected by a rotary switch.

Power Control

The primary power source for the computing system is 230 volts, 3-phase 60-cycle. A motor generator set is used to convert this voltage into the primary dc vol-

tages: +250, +200, and −160. These are fed to the power control unit and stabilized by electronic series field control action. The power control unit develops several other secondary voltages used in the system.

The primary windings of the filament transformers receive their power from a 230-volt single-phase voltage regulator. These transformers are mounted on both sides of the computer cabinet and are separately fused.

The power for the system averages 15.2 kva exclusive of the IBM units. The dc voltages used are +250, +200, +170, +67, −12, and −160 with respect to ground. These voltages are all regulated within 1 per cent including warm-up drift, with the power control retaining full regulation over a variation of 15 per cent for testing the equipment. All voltages and currents are metered on the front of the power control cabinet. The voltage meters have limit switches for both the high and the low direction so that if temporary failure in any derived or primary voltage occurs, all but the filament, drum, and blower voltages are shut off in the main computer and auxiliary equipment cabinets, and a warning alarm is turned on. A series of automatic controls insures that voltages are turned on in the correct order.

Separate sections of the computer are individually provided with grasshopper type fuses which set off an alarm on overload and shut off all dc voltages, the fuse indicating where the overload occurred. Heater-to-cathode leakage currents are metered and will trip a warning alarm if they exceed 1 milliampere.

Logical Elements

As mentioned previously, information is handled throughout the machine in two different forms

1. As a pair of dc levels generated by a voltage present on the plates of a flip-flop.
2. As a 0.5-microsecond pulse generated by a blocking oscillator.

All logical operations take place as the conversion of one dc level to a second dc level, nominally 117 volts in the low, or zero, state and 168 volts in the high, or 1, state of the flip-flop.

Flip-flop

The flip-flop, in general, is used in three related ways: as a static shift register, as a logical element, and as a counter. One standard plug-in contains four flip-flops and eight cathode-followers for isolation. As used in registers, one plug-in unit contains one decimal digit. The units are identical regardless of their position or loading conditions, but for sections of a register which are heavily loaded, heavy-duty cathode-followers are used. For a schematic of a typical flip-flop and shifting arrangement, see Fig. 3. The flip-flop is quite straightforward in design and has been found in practice to be a stable, general-purpose element.

A feature of the flip-flop design is the use of isolating diodes in both grids, with the resistors returned from the cathodes of the isolating diodes to a constant dc source of 67 volts. Normally the higher grid rests at about 63 volts. The 4-volt bias across the diode effectively blocks noise pulses. Raising the 67-volt level in certain sections of the machine will give a good indication of safety margin in pulse amplitude. This margin can be checked while a problem is in operation in the machine. Special problems have been developed that give rapid checks of this nature and are internally self-checking, so that when a flip-flop fails, it is a relatively easy matter to check the program and determine the exact location of the flip-flop that is apparently getting

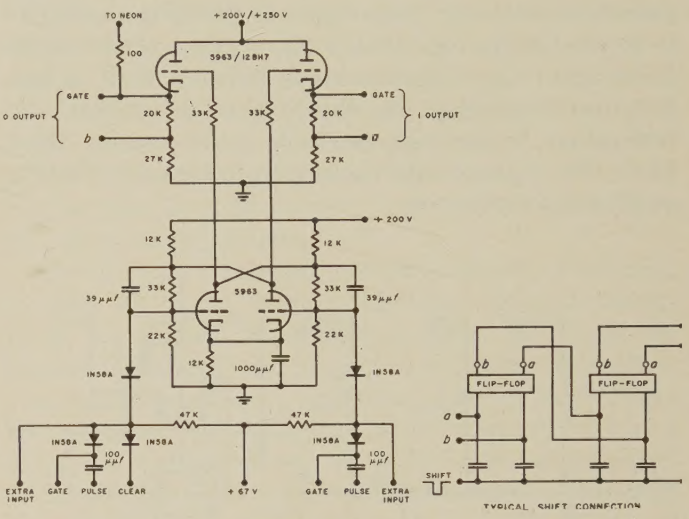


Fig. 3—Flip-flop circuit.

pulses of smaller amplitude than those of the rest of the circuitry. Similarly, as the 67-volt bias is lowered, the noise level increases and any large spikes or other interference can be located. One per cent deposited carbon resistors are used in all sections of the flip-flop circuit that determine the voltage levels so that, except for cathode-follower grid-to-cathode rise, an accurate level is maintained throughout the machine on voltages generated by the flip-flops. Register decades, to be accepted for machine service, must shift and circulate number patterns at a frequency up to 400 kc without error. Although the gates may not be capable of complete rise and fall at this frequency, depending upon load impedance on the output of the cathode-followers, the margin is such that correct operation can be extended up to this frequency. This gives a satisfactory margin over the speed at which the machine normally operates from the drum. A comparable test is also made when using the flip-flops as counting elements.

Blocking Oscillator

The second type of element for handling information is the blocking oscillator. Fig. 4 (next page) is a schematic of this unit. Unlike the flip-flops, the input gate circuitry in blocking oscillators operates over the full dc level range of the flip-flop output and inhibits or gates through pulses of positive rather than negative polarity.

The component values chosen are such that the blocking oscillator emits both positive and negative pulses 0.5 microsecond wide. Negative pulses are 30 volts, positive pulses 50 volts, in amplitude. Blocking oscillators were chosen initially because of their low output impedance and because of their proved ability to operate over wide ranges of loading and tube characteristics. This feature was of particular value in the early stages of design of the computer, since without modification the blocking oscillator could trigger several flip-flops, or other blocking oscillators, or entire registers, (44 flip-flops) with virtually no change in shape or amplitude of output signal. The rapid rise of the output pulse also permitted relatively long chains of blocking oscillators to be used in the logical networks with no serious delay in terms of the 7 microseconds between digit pulses. Extended operation has shown that no unusual deterioration in blocking-oscillator pulse output takes place. The highest duty cycle operated by any blocking oscillator is 7 per cent.

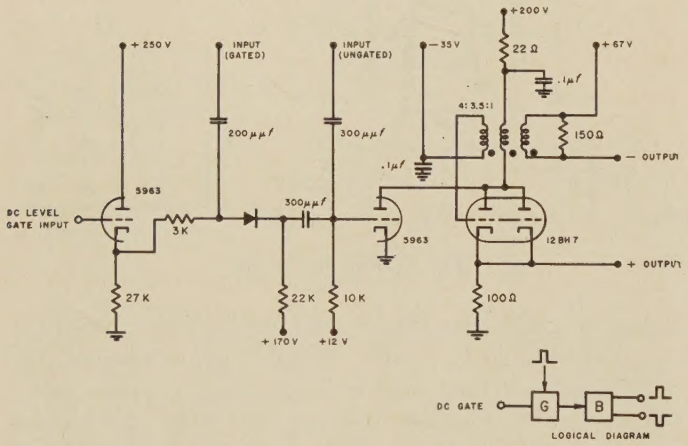


Fig. 4—Blocking oscillator schematic.

Machine Timing Cycle

The following description will outline the seven major steps the computer follows in performing the orders it receives in the command register. An understanding of these operations will make clear the manner in which the flip-flops and blocking oscillators work together to produce the desired logical transformations on data received from storage.

Timing pulses are derived pulses emitted in a fixed sequence by one of several control sections, at varying intervals which are multiples of a word-time, depending on the time required for the operation initiated by the timing pulse. The timing pulses are numbered consecutively TP1 through TP7 and the logical operation can be divided into the operations of fetching a command and executing the command fetched. The start pulse indicated in Fig. 5 is generated by a push button. If the timing flip-flop indicates that the next operation is to be a fetch, this pulse is emitted as a TP1 and goes to shift-control. At the same time, it sets the timing flip-flop to the "execute" state, so that when next a pulse returns to central control, it will be emitted as an execute pulse. The TP1 pulse now shifts the contents of the control counter into the address register, which tells the machine where in the storage it will find the next command. The pulse will be emitted by shift-control as TP2a and will go to memory control and set the coincidence circuit for the address held in the address register. Sector coincidence will be set up modulo 20 if the address is in a quick-access section and will be set up modulo 200 if the address is in main memory, thus locating the sector where the instruction will appear.

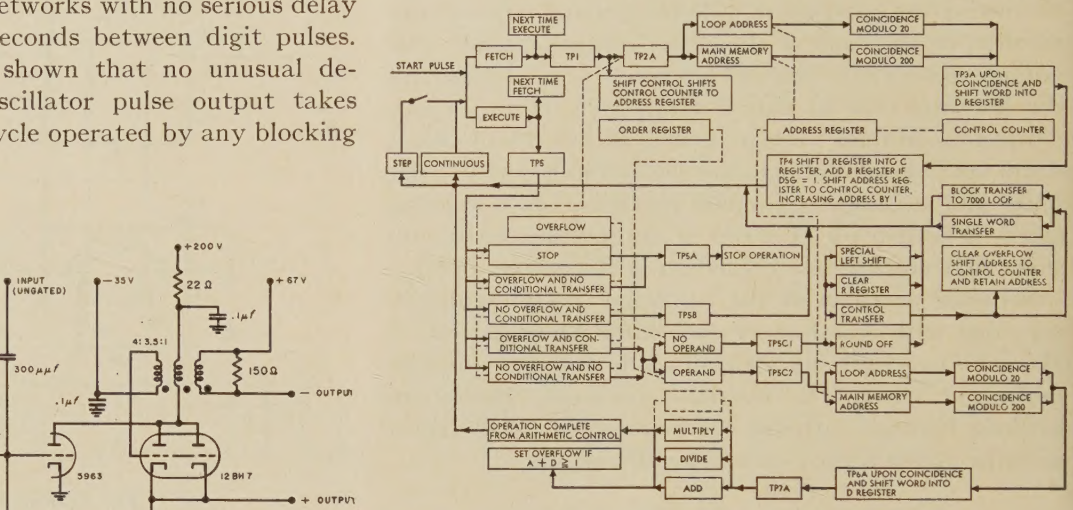


Fig. 5—Simplified central timing cycle.

At this time the appropriate band selection will also be made. Upon coincidence, the instruction will be transferred, starting with the TP3a, from the quick-access section or main memory to the D-register. TP4 is then emitted and transfers the contents of the D-register to the command register and at the same time initiates addition of the contents of the B-register to the address if the sign column of D contained a 1. The serial addition with which the contents of the B-register can modify the address is simultaneous with the shifting of the D-register into the order and address registers. An operation-complete pulse is then emitted by arithmetic control. This pulse finds the timing flip-flop in the execute state and sets it to the fetch state. The pulse then goes through other sections in central control. Here there are five possibilities, depending upon what is in the order register:

1. Stop order.
2. Overflow with no conditional transfer.
3. No overflow with conditional transfer.
4. Overflow with conditional transfer.
5. No overflow with no conditional transfer.

In the first two cases the machine will emit a TP5a, which gives an alarm and stops computation. If there

is no overflow but there is a conditional transfer, the machine must not execute the conditional transfer command but must go on to the next command, so a TP5b pulse is sent out as an operation-complete pulse, returns to the timing flip-flop, finds it in fetch, and then initiates the next fetch operation. If there is overflow and a conditional transfer is the next order fetched, or if there is no overflow and no conditional transfer, the machine emits a TP5c. If the 10's column of the order register contains a 1, 2, 3, 4 or 5, no reference to memory for an operand is necessary during execution. Orders of this type would include roundoff, special left shift, transfer to memory, etc. If no operand from storage is needed, the operation is immediately started by a TP5c1 pulse from central control sent to arithmetic or memory control by an appropriate blocking oscillator gated on by the order register. At the completion of the order, arithmetic or memory control emits an operation-complete pulse back to the timing flip-flop, finds it in the fetch state, and then initiates the fetch operation.

If the 10's column of the order register contains a 6 or 7, reference to memory for an operand is to be made during execution. Orders of this type include the arithmetic operations, setting the B-register, and sign comparison. Upon band selection and sector coincidence, TP6a is emitted and memory control reads the operand out into the D-register. One word-time later, the D-register contains the operand, and TP7a is emitted from memory control. Once again the order register is sensed to indicate which operation the machine is to perform. After the operation, whether one word-time later, as in sign comparison, or 102 word-times later for the multiplication of all 9's by all 9's, an operation-complete pulse is emitted by arithmetic control. This in turn is gated through into the execute-fetch section of central control, where the entire cycle is repeated.

It should be mentioned that the design of the computer permits asynchronous operation with respect to the drum after a word is shifted from memory into the D-register. Normally, the machine operates directly in synchronism with drum pulses. For testing arithmetic operations, however, it is convenient to operate the machine from an external oscillator at any frequency up to about 180kc. An explanation of this upper limit will be given in the discussion of the adder.

Magnetic Drum Memory

The magnetic drum is of conventional design. With the circuitry and heads used, the magnetic coating gives a minimum signal of $1\frac{1}{2}$ volts peak-to-peak. Twenty bands, each of four tracks, make up the main storage. Each band stores 200 words, making a total main storage of 4,000 words. Three timing tracks contain respectively a single pulse to serve as an origin pulse, 200 equally separated space pulses which occur in the one-digit interval between words, and a half-clock-frequency sine wave in phase with the origin-pulse and space-pulse tracks. This wave is frequency-doubled and appropriately shaped to serve as digit pulses, which are the working clock during normal operation.

A quick-access storage composed of four circulating read-record loops, each with a 20-word capacity, completes the drum storage. The quick-access storage is designed to block-transfer 20 words to or from any section of main storage or to transfer a single word to, or receive one from, the accumulator register. The quick-access sections are designated as the 4,000, 5,000, 6,000, and 7,000 sections, with the 7,000 section serving a rather special function which will be described later. Since each section has 1/10 the capacity of any band, the access time in a quick-access section is 1/10 that of main memory.

There are 2,400 bits (counting the spaces between words) on a single track around the drum, which is driven by a 3-phase motor at 3,550 rpm. The clock-frequency corresponding to this drum speed is 142kc, which gives an interval of 7 microseconds between bits. These figures indicate a maximum access time of 16.9 milliseconds in main memory and 1.69 milliseconds in the quick-access sections.

The heads are mounted in clusters of four. Each head is made up of two half-oval ferramic cores. After the cores are wound and joined in pairs, the heads are potted, assembled, and ground to a finished dimension. A pivot action allows a radial variation for each cluster to correct for any variations in the height of bosses on the drum housing and a cam action gives a circumferential adjustment of the heads. The heads are positioned to a distance of about 0.001 inch from the surface of the drum, which has been balanced and machined to a maximum eccentricity of 0.0002 inch. Fig. 6 is a photograph of the head assembly.

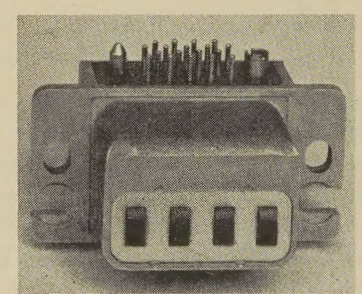


Fig. 6—Read-record head assembly.

A nonreturn-to-zero technique is used for recording on the drum. The surface is magnetized to saturation in either north or south polarity and the polarity of the flux changes only when the bit information is changed. Therefore, a signal, which is approximately the derivative of the record current, is read only when a change in bit information takes place. To enable the computer to distinguish between a track containing all ones and a track containing all zeros, a zero is always recorded between words. Thus, if there is no change in signal after space-pulse time, the track contained all zeros.

The recording tubes used in main storage are 5687's, which give a record current of 125-ma peak value. The quick-access section record tubes are 5881's, which are necessary because of the high duty-cycle and correspondingly higher plate dissipation. The record currents in the quick-access sections are about the same as in main storage.

As mentioned previously, electronic switching is used in the memory section. A high switching speed is necessary because of the block transfer to and from the quick-access section across the band-switching points in main memory. There are two rather difficult requirements in the read-record amplifier section of storage: First, it must be possible to read from one head and, within 7 microseconds (in between words), switch the read amplifier to a second head on the storage drum. Second, it must be possible to record with one head and, after three word-times, or about 250 microseconds, to read information with the same head without serious interference from transients. Fig. 7 shows the main-storage read-record switching circuitry to achieve proper band selection and read-record switching. When the head is recording, the appropriate bus is energized by the selection circuit, enabling the 5687's to record either a one or a zero. At the same time, the read amplifier, which is not shown in the figure, is gated off. When a signal is to be read, both of the record amplifier sections are biased off and the signal appears on the grids of the two 5965's shown at the right. The useful head signal is the difference voltage between the grids. By using transformer coupling in the cathode-followers, this difference voltage is effectively obtained and the square-wave gate voltage is cancelled except for small spikes at the amplifier input corresponding to the leading and trailing edges of the gate voltage. The gating transients have subsided at strobing time in the read amplifiers.

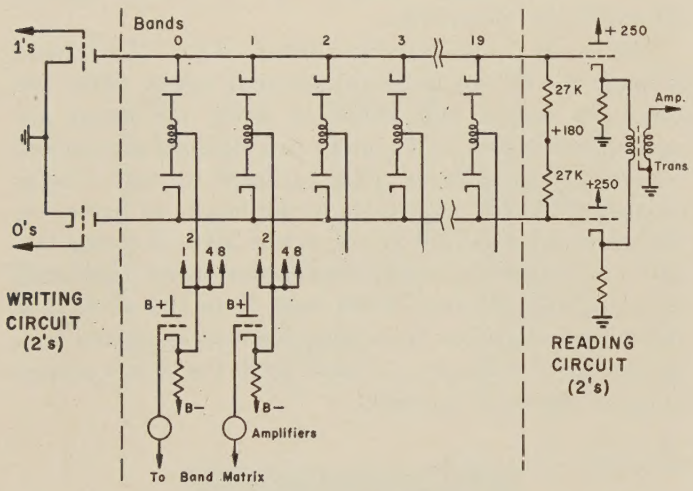


Fig. 7—Memory read-record switching circuitry.

To make optimum use of the quick-access storage and to effectively increase the machine speed by reducing access time, a special command is used for the operation of the 7,000 quick-access section. Normally, operands are block-transferred to the 4-, 5-, and 6,000 sections, and commands are block-transferred to the 7,000 section. Several commands permit a conditional or unconditional change of control to transfer the contents of main-storage locations x through $x+19$ into the 7,000 section, where the address correspondence is modulo 20. The computer immediately begins executing the command which came from memory location x and then, unless there is a change of control, proceeds to the next command in the 7,000 section. This technique permits maximum use of the quick-access storage and increases the operation speed of the computer by a factor of about 7, in most cases, over that obtained from main storage alone. The circuitry for quick-access storage, main storage, and memory control uses a total of about 450 vacuum tubes.

Order List

The following brief description of the order list places emphasis on those orders that are out of the ordinary.

Addition and subtraction may be performed algebraically or with the absolute value of the addend or the subtrahend and may include preliminary clearing of the A-register, or not, as ordered. Multiplication gives either a 20-digit product or a 10-digit rounded product. Division of the 20-digit number in the A- and R-registers by a 10-digit divisor gives a 10-digit quotient in the A-register and a 10-digit remainder in the R-register. The 20-digit number in the A- and R-registers, excluding the sign, may be shifted or rounded off. A circulating left shift of the A-register, including the sign, is provided to permit the handling of digits other than 0 or 1 in the sign column of the A-register as a convenience for special operations. The R-register, which is normally an extension of the right end of the A-register and is used for double precision operations, may be separately cleared. An extract or logical multiplication order is provided for alteration of instructions.

Orders to effect branching operations include the following:

A zero check order will transfer control to any assigned memory location if the content of the A-register is not zero; otherwise, of course, the computer goes on to the next command in sequence.

A sign compare order sets the overflow flip-flop if the sign of the number in any selected memory location is not the same as the sign of the number in the A-register. Setting the overflow flip-flop is the standard technique to effect a conditional transfer of control from one instruction to another out of sequence and is described in the Machine Timing Cycle section.

To facilitate re-entry into a main routine after completion of a branching routine, the address of the next instruction for re-entry can be automatically stored before starting the branching routine.

The address part of any command tagged with a minus sign has the contents of a special four-digit register, the B-register, added to it just before the command is executed. The command is not changed on the drum, so that operands can be called from memory with no need to restore or prestore the addresses. A whole group of commands (each marked negative) requiring address alteration can be altered by one B-register command. The 4-digit number held in the B-register can be counted down or up by computer orders or have its contents changed to any assigned number less than 10,000. When counted down, it acts as a change-of-control command on zero in the B-register and branches to any assigned memory location. It can also be used with input from the photoelectric reader to alter addresses within subroutines so that these subroutines may be placed at any point in the memory.

Information may be transferred from the A-register to any memory location, with or without retaining the contents in the A-register. Also, block transfers of 20 words can be made from quick-access storage to main memory or the reverse.

To aid the programmer in floating point operations, the number in the A-register can be normalized and the number of left shifts tallied in a special counter. If the A-register was clear before the operation, control is transferred to a preassigned memory location.

Suitable orders are used to shift information in and out, from and to the appropriate input/output devices. A special order adds a single digit to the accumulator when a key on the decimal keyboard is pressed. This in effect gives the operator a branching order with 10 terms instead of 2, and depending on his judgment rather than on a machine decision.

Adder Section

All arithmetic operations and most logical operations are controlled by the arithmetic control section which, in turn, receives its start operation pulse from central control. The basic function of the arithmetic control is to emit pulses to shift information to and within appropriate registers and the adder column and to supply the serial decimal adder with properly timed pulses. The adder is used in 19 out of the 55 operations the computer can perform and affords a good example of the engineering and logical techniques used throughout the machine. See Table I for an outline of its operation.

Addition is performed serially on the decimal digits and can be divided into four basic operations performed in the following order:

1. Nines-complement the adder column if necessary.
2. Add the digit in D-10 (least significant digit in the D-register) to the adder column and carry flip-flop, leaving a binary sum in the adder, including a base-16 carry, if any.
3. Change the binary sum in the adder column to a decimal sum including a base-10 carry, if any.
4. Shift the contents of the adder column (but not the decimal carry) into the sign column of A and at the same time shift the D- and A-registers one step right, with A-10 (least significant digit in the accumulator) going into the adder column.

In addition to this basic cycle, the following operations are necessary. The sign columns of the A and D registers are compared and if they are found to be different, the adder column is nines-complemented and the carry flip-flop is set to 1 before the first add operation to make a true tens complement of the A-register contents. The sign of the D-register is shifted to the sign flip-flop. To enable the computer to discriminate between the negative sign and the 1 which an overflow produces at the end of an addition, the signs of both A and D are cleared before the addition. The sign of the 10-digit sum is set as indicated in Table I. Since the sum appears in complementary form if the signs are different and if A is greater than D in absolute value, some additions require a second 11-digit add cycle during which the A-register is again complemented and added to 0 in the D-register. Such an addition takes four word-times—340 microseconds. About one-fourth of all additions performed will be four word-time additions, so the average addition takes 2.25 word-times, or about 190 microseconds. Fig. 8 (next page) is a diagram of actual pulse timing for a two-word-time addition.

TABLE I

Rules for Addition

Before the add operation

Arithmetic Order	*Sign of D-Register*
add number	leave unchanged
subtract number	reverse
add magnitude	set to 0
subtract magnitude	set to 1

Transfer the sign of the D-register resulting from the choice above to the sign flip-flop and then clear the signs of both the A- and D-registers.

During the add operation

Signs of A and D Before Clearing	*Form of Digits from A to Adder*
same	unchanged
different	tens complement

Add decimal digits serially right to left, including the cleared sign digits, shifting the sums from the adder through the sign of the A-register, leaving the sum in the A-register.

After one register-length add operation

Digit in Sign Position, A-Register	*Operation*
0	Transfer the content of the sign flip-flop to the sign of the A-register. Arithmetic order is complete.
1	Indicate an overflow, since the sum is unity or greater. Adjust the sign of the A-register and hold the fractional sum.
9	Repeat the add cycle, complementing A, which is added to 0 in D, since D is cleared by add cycle. Adjust the sign of the A-register.

Fetching a command and an operand from the quick-access storage requires two mean access times, or 1.7 milliseconds. The figure used to estimate computing time is 2 milliseconds per operation—which comes quite close in programs long enough to average out the operations, excluding multiplication and division. These average an additional time of 6.5 milliseconds and 10 milliseconds respectively.

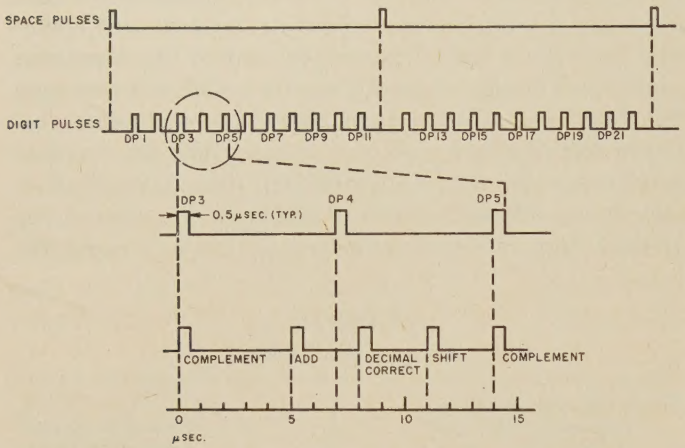


Fig. 8—Adder pulse details.

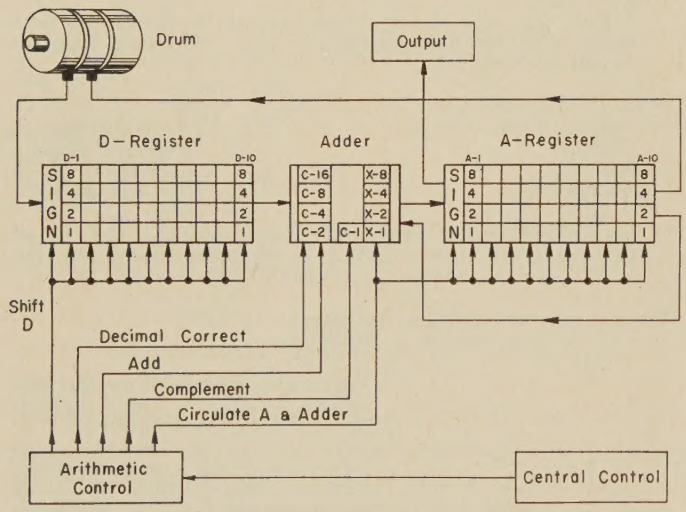


Fig. 9—Information flow during addition cycle.

The adder (see Fig. 9) is actually four binary adders wired to operate in time-series. After the adder column has or has not been complemented by the gated blocking oscillator complement pulse from arithmetic control, the gate circuitry is allowed 5 microseconds to settle before the add pulse is emitted. During this interval, if the lowest-order binary sum has a binary carry, a carry inverter (a dc operated flip-flop) is "pulled" (rather than triggered) to its 1 state. This level, together with D10-2 and X-2, determines whether C-4 is pulled to its 1 state, and so on up to C-16. If C-16 is pulled to its 1 state, the add pulse is then gated through and sets the carry flip-flop, indicating a base-16 carry. When the decimal-correct pulse is emitted by arithmetic control, the adder column and the base-16 carry are converted to a decimal sum and a decimal carry.

This design provides decimal output and the simplicity of a binary adder without a large number of components. The adder operates reliably over a frequency range from single-pulse operation to about 180kc. This upper limit is set by delays between the complement and add pulses and between the decimal-correct and shift pulses, which are fixed by delay lines. Therefore, at 180kc, or a period of 5.56 microseconds, a rise in frequency over the range 142 to 180kc disproportionately diminishes the undelayed pulse intervals. These are from add to decimal-correct, and from shift to complement. Normally about 3 microseconds, they are reduced by a 180-kc clock rate to 1.56 microseconds, which approaches the resolution time of the gate levels. These are considerably more complex than those required for straight shifting and so require longer to stabilize. Thirty-one twin-triodes and 71 crystal diodes are used in the adder section, excluding pulse-mixing diodes in the adder input.

Computer Maintenance

The following description briefly outlines some of the facilities that have been designed into the equipment to minimize downtime. Their functions are to indicate failute, to locate failure, and to induce failure in sections that are becoming marginal.

Failure Indication

An alarm light is turned on and computation is stopped by a forbidden combination (binary 10 through 15) appearing in the least significant decade of the A-, B-, D-, and R-registers, the address register, the control counter, and the shift counter. Inspection of the register contents as indicated by the neon lights indicates the failure location.

A sector alarm will stop machine operation if the sector counter does not contain 0 at the time the origin pulse is read, once per drum revolution. This check prevents information from being recorded on or read from incorrect sectors of the drum for more than one drum revolution.

An audible alarm indicates excessive rise in exhaust air temperature in the computer cabinet and after a preset interval up to 15 minutes, dc voltages will be shut off if the temperature stays at or above a predetermined level.

Marginal Checking and Aids in Locating Failure

A built-in test oscillator plug-in gives a variation in digit frequency in four steps from the nominal 142kc down to where each pulse is applied by pressing a button. Also, an external test oscillator may be incorporated for continuous variation of clock frequency from the upper limit of approximately 180 kc down to 20 cps operation. The external oscillator provides a convenient

means of operating the control section of the computer at a raised frequency and thus showing up by specific failure any gates that are slow during certain operations of the machine. If data are kept on the specific problem and the failure frequency for this problem over a period of several months, the long-term stability of the machine can be accurately checked. This technique can be used to show up slowly changing characteristics such as resistor drift, forward- and back-resistance changes of crystal diodes, and severely lowered emission from blocking oscillator tubes.

The ungated input of the blocking oscillator may be pulsed with a double pulse generator with variable separation between pulses (0 to 10 microseconds) and variable pulse repetition frequency (0 to 1 kc). During certain marginal checks, this technique has the advantage of giving the equivalent of step operation for convenient observational check, while at the same time allowing the pulse pairs to exercise the circuitry for short intervals of time at a rate that may exceed the normal clock frequency.

A third technique that has been found of value is the lowering of individual pulses at specific points in the input to each blocking oscillator. Test points are brought out to the front of the blocking oscillator package. These points serve two purposes: First, they make the signal easily visible with an oscilloscope from the computer front. Second, they facilitate lowering the amplitude of the pulse at selected points. This can be done conveniently by taking a test capacitor and shunting to ground each blocking oscillator test point in turn. This indicates specific pulse amplitudes that are marginal during the operation of a self-checking problem. If a pulse falls below a minimum value and causes failure, the machine will stop after the self-checking portion of the program. By lowering the 12-volt bias in a selected group of blocking oscillators, the positive amplitude of pulses gated into the blocking oscillator can be effectively lowered, and thus a more general rather than an individual check of margin can be made.

Special systems provide reductions in tube heater voltage to induce marginal errors in sections of the machine that may be nearing the failure point. With the flip-flops used, it has been found convenient to lower either one or the other half-section of each filament in a selected section of flip-flops, with all flip-flops resting in either the 1 or 0 position. After the filament temperature has stabilized, if the flip-flop tube is marginal, it will often have a preference for either 1 or 0, as indicated by the neons on the supervisory control panel. In this manner flip-flop failure can be detected before it actually causes machine error. Variations in the bias with respect to the amplitude of pulses entering the flip-flop have been previously described.

Special circuits are provided for rapid checking of individual parts of the computer. A few of them are:

Recycle Switch: When the recycle switch is used, internal storage is effectively eliminated from machine operation. This provides a quick means of checking the arithmetic and control portions of the computer. If an add test is to be made and storage is not to be used, one operand is placed in the D-register by push buttons and the second operand is placed in the A-register in the same way. The operator then sets up the command "add hold" in the command register and depresses the *step* button, which causes a complete addition of the A- and D-registers to be performed, leaving the sum in the A-register for visual check. With this technique, there can be no doubt whether the proper number was switched from storage into the D-register to perform the addition, since storage is completely eliminated.

Circulate D Switch: By circulating D, the operator can perform continuous sums in the accumulator and thus get a relatively quick check with the sum in the accumulator being changed each time an operation takes place.

Command Complement Switch: This switch is another means for a quick check of the control circuitry operation. It converts a command from an even to the next odd number or the reverse after the completion of each operation. For example, the order number for multiply is 60 and for divide is 61. Now, once again the operator sets the recycle switch so that memory is not used, puts an operand in the A-register and one in the D-register and puts a 60 in the order register to instruct the machine what operation it should follow. With the command complement Switch in the "on" position he then pushes the step button and the machine performs a multiplication. At the same time, the order in the order register is changed to 61. If he pushes the button a second time, a division will then be performed and the quotient will appear in the A-register with, of course, a 0 remainder in R. At the conclusion, the order register will once again contain 60. Pressing the continuous button at this point affords a convenient means of operating the machine continuously, multiplying and dividing this particular set of numbers. If the machine makes an error in the multiplication or division, a wrong answer will show in the A-register when the machine is stopped.

Construction Details

In the design and packaging of the equipment, considerable effort was made to mount most components on easily removed, pluggable chassis of uniform design and yet keep the number of unused or redundant components down to a minimum. An 8-tube basic unit was chosen as the best compromise from an economic standpoint. At the same time, this arrangement allows the wire and connector-pin capacitance to be held down to a reasonable value, thus avoiding unduly high power consumption to maintain gate rise and fall times. Fig. 10 (next page) is a photo of a typical plug-in chassis. On each chassis are two 32-pin connectors that give a low-friction wiping action permitting the plug-in to be easily inserted. The plug-in handle guides and centers the

unit properly before the connectors make contact and supports it after it is locked in place with a detent action. The plug-ins are mounted in the front section of the computer cabinet for easy access.

Ambient air is used for cooling and passes through filters at the ends and rear of the lower cabinet section, through centrifugal blowers into a plenum chamber immediately below the plug-ins. It circulates at uniform pressure and distribution throughout the length of the main cabinet up through the plug-ins and exhausts out the top of the cabinet. The air may be exhausted directly into the room, if sufficient air conditioning is available, or may be ducted to the outside. The cabinet doors may be left open for servicing without seriously impairing the cooling of the computer.

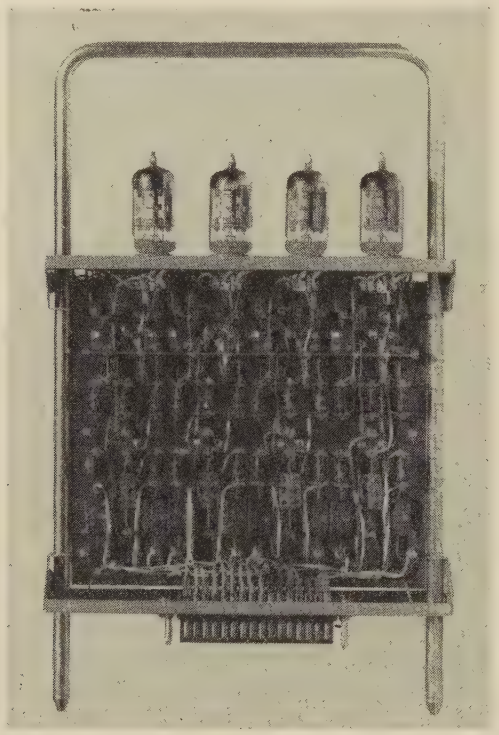


Fig. 10—ElectroData plug-in chassis.

The main cabinet is 143½ inches long, 28 inches deep, and 78 inches high. The console is 30×60×30 inches; the power control cabinet is 24×28×78 inches; the punched card converter is 56×28×67 inches. The computer cabinet is constructed to permit separation along a vertical plane to the left of the storage drum in case freight elevators, sharp-angled corridors, etc. are too small to admit it.

The internal cabinet wiring falls into three general classes:

1. Power
2. Dc level
3. Pulse.

The dc power buses are routed along the front side of panels supporting the base connectors for the plug-ins,

Fig. 11—ElectroData computer—rear view.

with the terminals of decoupling capacitors acting as tie-points for the power leads before they go into the base connectors. The filament buses are copper straps, 5/16×3/64 inches, that are cast in a polyester to give a high-conductance multi-conductor bus of relatively small cross section. To help reduce wiring capacitance in long runs in the gate lines, the dc levels are run along spaced wires, as shown in Fig. 11.

The pulse lines are twisted-pair wires, laced into cables, and since the pulses are developed in relatively low-impedance circuits, cross-talk between the twisted-pair wiring is negligible.

A total of 173 plug-ins of 23 different types is used in this system. However, the two main types previously described, the flip-flop package and the blocking-oscillator package, account for 58 per cent of the total. The number of tubes of each type used in the system described is as follows:

Tube Type	*Quantity*
5963	558
12BH7	430
5965	253
2D21	92
5881	70
6AN5	42
5687	39
6AS7	20
6AU6	11
OA3	4
OB2	2
OC3	2
OD3	2
Total	1,525

The tube count averages more than eight tubes per plug-in because the power control cabinet contains no plug-ins and the punched card converter has a number of tubes not mounted in plug-in assemblies.

The germanium diodes used are tested for specific characteristics and are all of one type. Their characteristics are similar to those of a standard 1N65. The system described uses a total of 3,809 diodes.

Transistor Circuitry for Digital Computers*

C. L. WANLASS†

Summary—**Transistor circuitry is presented that enables the construction of a digital computer which will operate at a clock frequency of 200 kc or less. The circuitry employs readily available germanium or silicon junction transistors of the type used in audio-frequency circuit work. A new system of diode gating is also presented as a necessary part of the circuit philosophy. No vacuum tubes are required or used within the computer.**

Introduction

THERE HAS been much said about the duality existing between the vacuum tube and the transistor. However, it becomes evident in many cases that a very complex circuit is present when one adapts the practices of vacuum tube circuitry and applies them to transistor circuitry. The art of becoming familiar with the element with which you are working can never be replaced by the art of duality with another element.

It is interesting to note that the transistor actually adapts itself more readily to digital computer circuitry than does the vacuum tube. The mere fact that *n-p-n* and *p-n-p* transistors exist is one attribute peculiar to the transistor that is extremely helpful in designing computer circuitry. In addition, the problem of packaging transistorized equipment is much simpler than that of packaging equipment employing vacuum tubes.

This paper presents circuitry necessary for design and construction of a computer using available components operating at 200 kc or less. The system employs a magnetic disc as main internal storage. The remainder of the machine, including read-in and read-out of the memory, makes use of transistor and diode circuitry. No vacuum tubes are used within the machine.[1]

Logical Gating System

In formulating a system of diode gating for use with digital computers employing transistor flip-flop circuitry, it is important that the characteristics of the transistor be a dominating factor in the diode gate design. Because of this reliance on transistor characteristics, an attempt was made to use a system of gating that gates information in such a manner as to keep the average power requirements low. In an attempt to keep the average power requirements of the gating low, some type of pulse gating is necessary. Thus the gating system developed for previous vacuum tube computers seemed ideal because of its use of "dc pulse" gating. In fact, it was to some extent the availability of this "dc pulse" gating that first made the use of transistor circuitry in a computer a practical venture. Because of its many advantages, "dc pulse" gating was adopted for use in the transistor computer. The gating system employed is shown in Fig. 1. The logical equations which will be used to explain the gating operation are presented below:[2]

$$ {}_1a_1 = BD'E + FGH $$
$$ {}_0a_1 = I'JK + LM'N. $$

In the above Boolean equations, the capital letters refer to flip-flop circuit outputs and the lower case letters refer to flip-flop circuit inputs. The subscripts preceding the lower case letters indicate the state to which the flip-flop circuit under discussion will be set if the logical equation is equal to 1 and a clock pulse occurs.

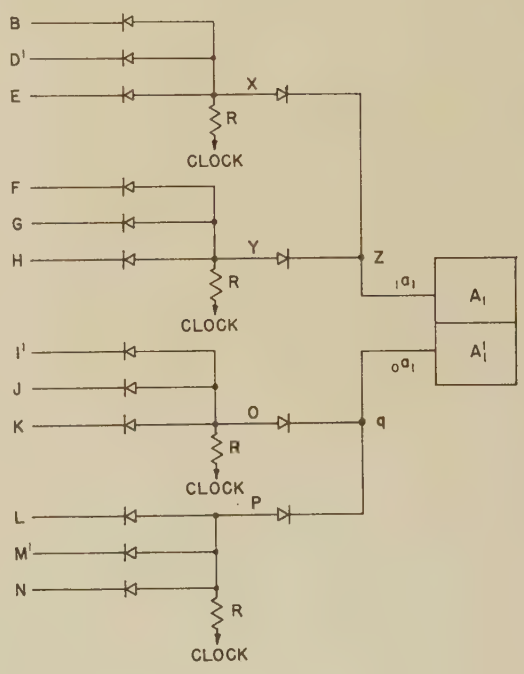


Fig. 1—Logical gating system. All diodes are Type IN99. $R = 20$ k.

The subscripts succeeding the lower case and upper case letters are used for identification purposes. It should also be pointed out that the primed terms are the complements of the nonprimed terms.

Operation of Gating Circuitry

Assume the following:

1. E_L equals the lower voltage state of the flip-flop;

* Original manuscript received September 15, 1954; revised manuscript received December 9, 1954. This report refers to work done while the author was associated with North American Aviation, Inc.

† Ramo-Wooldridge Corporation, Los Angeles, Calif.

[1] Such a machine is under construction at North American Aviation, Inc., Downey, California.

[2] E. C. Nelson, "An algebraic theory for use in digital computer design," *Trans. I.R.E.*, vol. EC-4, pp. 12–21; September, 1954.

this corresponds to the 0 state of the flip-flop circuit.

2. E_H equals the higher voltage state of the flip-flop; this corresponds to the 1 state of the flip-flop circuit.
3. The clock pulse, C, is a positive pulse and is normally returned to the potential of the low state E_L, minus sufficient bias voltage to cut off all diodes during the dormant state or between clock pulses of the computer.

The operation of the gating circuitry is such that information is continually presented by the flip-flop circuits to the diode gate inputs. This gate input information is transferred through the diode gates to the input circuitry of the selected flip-flop circuits upon generation of a clock pulse. The result is that gating power is dissipated only during the time when the computer clock pulse is present. Therefore, the average power consumed per logical and-or gate is low for a comupter operating at a clock frequency of a few hundred kilocycles per second or less. Consequently a large number of diode gates may be connected to the output of each flip-flop circuit.

Complex Gating Combinations

Many times it is beneficial to cascade diode gates and form such combinations as and-or-and-or and even more complexed logical gating combinations. Conventional dc gating techniques require that the gating current increase as the number of and-or terms in the gate increase. In fact, the input to an and-or-and gate usually requires more than twice as much current as the input to an "and" gate. Because of this current increase as the logical gating is cascaded, the author does not recommend cascading to any extent in the conventional dc gating system. However, if a system of gating could be used that did not require this additional current when cascading, it is believed that cascading of diode gates would actually be beneficial in some instances because of the reduction of circuitry and gating power that cascading allows. Such a gating system is realized in the dc pulse gating system. The dc pulse gating system requires approximately the same amount of gating current for the and-or-and-or combination and more complex combinations as it does for the simple and-or combination. For reasons of example, the following and-or-and-or-and-or equation is mechanized in diagram form in Fig. 2:

$$_1s_1 = \{[(AB + DE)HI + (DE + FG)NO]JK + LM\}C.$$

It should be noted that the complex gating mechanization of the above equation requires 24 diodes, while the use of only the and-or combination requires 31 diodes, or 29 per cent more diodes. It is estimated that an overall reduction in the number of diodes of approximately 15 to 25 per cent is realizable when employing more complex gating than just the and-or combination. It is also believed that the use of more complex gating than the and-or-and-or combination is usually not necessary and should be avoided if possible, since effects such as stray capacitance and diode forward-voltage drop begin to play an important part in reliability as the gating becomes more complicated.

As would be expected, this gating system requires very low average current drain from the output of the flip-flop circuit. However, if a large number of diode gates per flip-flop output are to be driven, the peak diode gating current may be quite high. Thus a flip-flop circuit that provides a very low output impedance to a narrow clock pulse is needed.

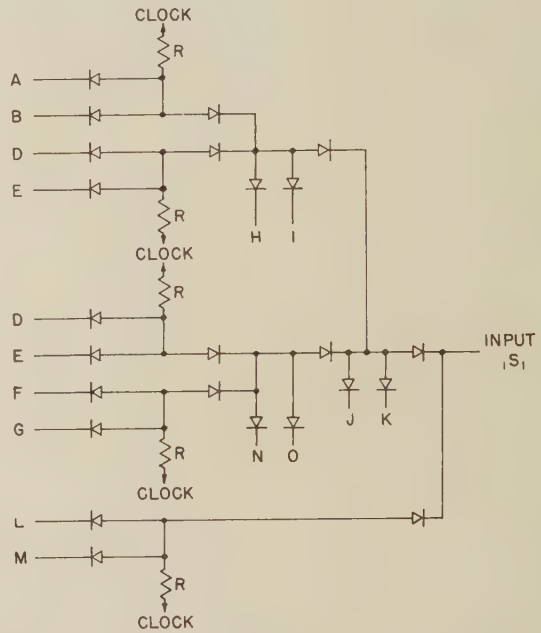


Fig. 2—General logical gating system. All diodes are Type IN99. $R = 20$ k.

Junction or Point Contact Transistor

In deciding on the transistor flip-flop circuit, the first decision required is whether to use a point contact transistor or a junction transistor as the active element in the circuit.[3] Because of the superior availability and reliability of the junction transistor, this unit was used rather than the point contact transistor. Having decided upon the type of transistor, the next and major problem of acquiring a low output impedance from the transistor circuit presented itself.

Low Output Impedance

It became evident after some consideration that one method of obtaining a low output impedance to a narrow pulse would be to store the flip-flop circuit output information or output voltage in some type of passive element. Since this passive element could deliver the required energy upon demand without relying on the

[3] Richard F. Shea, Ed., "Principles of Transistor Circuits," John Wiley and Sons, Inc., New York; 1953.

fast transient characteristics of the output transistors of the flip-flop circuit, this system seemed ideal for use with a junction transistor flip-flop circuit. Consequently, this type of flip-flop output circuit was adopted. The flip-flop circuit developed and in use at the present time is shown in Fig. 3. (It is noted that storage of information takes place in capacitor C_2. These capacitors have actually been made as large as 0.01 microfarad for a machine operating at 100 kc and using commercially available junction transistors of the audio-frequency type.)

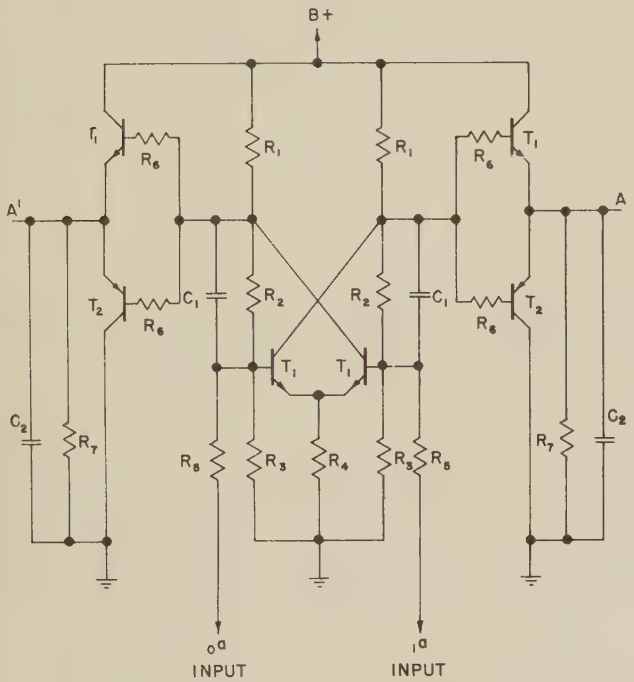


Fig. 3—Transistor flip-flop circuit. $R_1=15$ k, $R_2=150$ k, $R_3=56$ k, $R_4=1.5$ k, $R_5=3.9$ k, $R_6=2.4$ k, $R_7=50$ k; $C_1=68$ $\mu\mu$fd, C_2 depends on load; T_1 is a Texas Inst. Type 202 NPN, T_2 is a Texas Inst. Type 301 PNP.

To illustrate the operation of the output circuit, let us assume a clock pulse width of $\frac{1}{2}$ microsecond duration and an allowable increase in flip-flop output voltage during the gating process of three volts across the output capacitor. Using these conditions, the following gating currents can be delivered to the gating diodes during the clock pulse:

$$I \text{ output} = \frac{C\Delta E}{\Delta T} = \frac{3 \times 0.01 \times 10^{-6}}{0.5 \times 10^{-6}}$$

$$= 60 \times 10^{-3} = 60 \text{ MA}.$$

If, in turn, it is assumed that the gating current per gate is one ma, this means that 60 diode and-or or more complex gates may be driven per flip-flop circuit output at a rate of 100 kc. (It should be stated that 300 such gates have been driven at a rate of 50 kc and that 100 gates have been driven at 100 kc using a $\frac{1}{2}$-microsecond clock pulse and a capacitor size of 0.03 and 0.01 microfarad respectively.)

Transistor Current Requirements

One of the main advantages of the circuit is that the capacitor is actually charged or discharged during the time between clock pulses or over a 20-microsecond period in the case of the 50 kc machine. This means that the approximate maximum average current of the transistor driving the output capacitor is as follows: Assume a 10 volt logical flip-flop voltage swing and a 50 kc clock pulse frequency.

$$I \text{ av.} = \frac{C\Delta E}{\Delta T} = \frac{0.1 \times 10^{-6}}{40 \times 10^{-6}} = 2.5 \times 10^{-3} = 2.5 \text{ MA}$$

$$C = .01 \ \mu\text{fd}.$$

A ΔT of 40 microseconds was used in determining the maximum average transistor collector current because a given power amplifier either charges or discharges its load capacitor, but not both. In other words, an *n-p-n* transistor charges a given load capacitor and a *p-n-p* transistor discharges this same capacitor. It should also be pointed out that the above average current assumes the flip-flop to be changing state at the maximum rate. Naturally, very few flip-flop circuits in a given machine will be required to constantly change state at the maximum rate. Consequently, very few transistors will be required to deliver even this low value of average collector current.

Collector Dissipation

Another item of interest is the maximum average collector dissipation that a given transistor will be required to dissipate. If the assumption is made that the transistor acts as a current source in charging the capacitor, the dissipation is approximately

$$P \text{ av.} = \frac{2.5 \times 10^{-3} \times 10}{2} = 12.5 \text{ milliwatts}.$$

This power dissipation also assumes the flip-flop circuit to be changing state at the maximum rate.

Thus both the collector current and collector dissipation are well within the limits of almost any junction transistor. It can also be seen that with available low-power transistors it is possible to reach 300 diode gates per flip-flop output at 50 kc.

Flip-Flop Circuit Input System

The system used to couple information into the flip-flop circuit is unique and probably should be briefly explained. As can be seen in Figs. 3–6 on this and the following pages, a resistor is present between the base of the transistor in the flip-flop circuit and the output of the diode gating circuit. This resistor serves to allow the flip-flop circuit to which it is connected to be triggered when the diode gate output voltage is equal to that of the 1 state or high state of the system. The resistor also has the task of preventing the circuit from triggering when the diode gate output voltage is equal to that of the 0 state or low state of the system. Because of these

two functions that this series resistor performs, it is referred to as the "distinguishing" resistor.

Since the collector of a conducting *n-p-n* transistor can never become equal or less in potential than the base element of that transistor, and since the gating system being used is direct-coupled, it is evident that a positive pulse will be presented to each flip-flop circuit input during every clock pulse of the computer. However, the input pulse will be much greater in amplitude if the gate output potential is equal to the potential of the 1 state, than if the gate output potential is equal to the potential of the 0 state. The statements below indicate the available trigger current for the 1 and 0 states of the gating system for a practical case.

Assume:

I_R = Required trigger current.
I_T = Current input to a given flip-flop circuit when the diode gate output voltage is equal to the voltage of the 1 state.
I_F = Current input to a given flip-flop circuit when the diode gate output voltage is equal to the voltage of the 0 state.
E_G = Ground or reference potential = 0 volts.
E_H = Higher potential or the potential at the 1 state = 12 volts.
E_L = Lower potential or the potential of the 0 state = 2 volts.
R_d = Resistance value of distinguishing resistor.
R = Function of input resistance of the flip-flop circuit.

Let $I_T = 2I_R$ for safety, and

$$I_T = \frac{E_H - E_G}{R_d + R} = \frac{12}{R_d + R}$$

$$I_F = \frac{E_L - E_G}{R_d + R} = \frac{2}{R_d + R}.$$

Therefore

$$I_R = \tfrac{1}{2} I_T \text{ Safety factor of 2}$$

$$I_R = 3I_F \text{ Safety factor of 3}$$

$$I_T/I_F = 6 \quad \text{(distinguishing factor)}.$$

Naturally, the resistance of the distinguishing resistor may be set at a value to give optimum I_T/I_R and I_R/I_F ratios for a given piece of equipment.

Flip-Flop Circuit for Light Loads

Many times, a flip-flop circuit does not need to be able to drive more than a few diode gates. For these cases, it is possible to use only an *n-p-n* transistor to charge the output capacitor and a resistor from the emitter of the transistor to ground to discharge the capacitor. The circuit for light loads is presented in Fig. 4. Naturally, the output capacitors for the circuit of Fig. 4 are smaller in value than those of the circuit of Fig. 3 for any given maximum operating frequency.

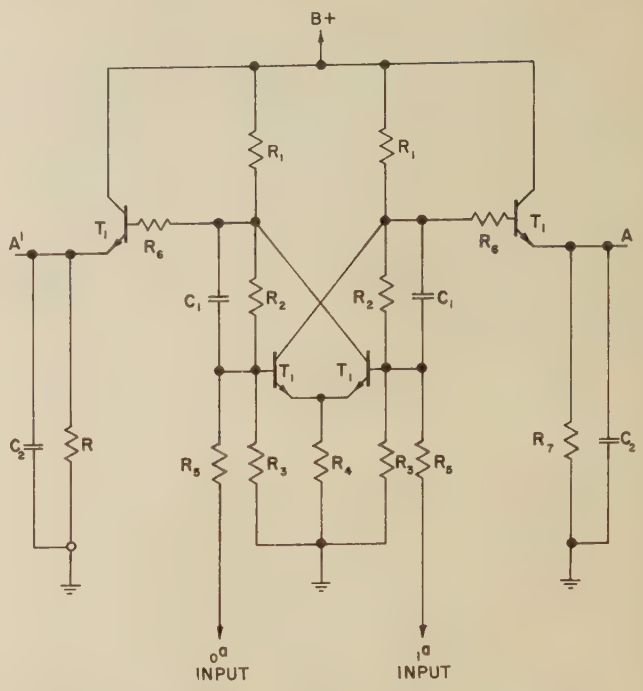


Fig. 4—Transistor flip-flop circuit for light load. T_1 is a Texas Inst. Type 202 NPN, $R_1 = 15$ k, $R_2 = 150$ k, $R_3 = 56$ k, $R_4 = 1.5$ k, $R_5 = 3.9$ k, $R_6 = 2.4$ k, R_7 and C_2 depend on load.

Flip-Flop for Low Clock-Pulse Frequency Operation

In cases where the flip-flop circuits are required to operate at a low maximum frequency, it is possible to remove both the *n-p-n* and *p-n-p* transistors that charge and discharge the output capacitor, and allow the flip-flop circuit itself to do the charging and discharging of the output capacitor. Removal of the capacitor-charging transistors is possible since the output capacitor is charged or discharged over a much longer period of time when a low operating frequency is used. Therefore, the average charging current is greatly reduced for a given value of capacitance. The circuit for low frequency operation is presented in Fig. 5 (facing page).

Write Amplifier

In addition to the circuitry so far presented, it is evident that a computing system using a magnetic disc for main internal storage needs some type of circuitry that will record on the magnetic disc. The circuit that usually accomplishes this recording task is referred to a a "write" amplifier or "write" circuit.

In an attempt to keep the different types of circuits to a minimum and to use only dc pulse gating throughout the computer, it was decided that a write amplifier that could be triggered like an ordinary flip-flop circuit would be beneficial. This type of triggered write amplifier would, of course, be ideal for use in a digital differential analyzer because the recirculation properties of a digital differential analyzer require that each recording head of the magnetic device be recording either a 1 or a 0 at all times when the computer is operating. The write circuit developed is presented in Fig. 6 (facing page).

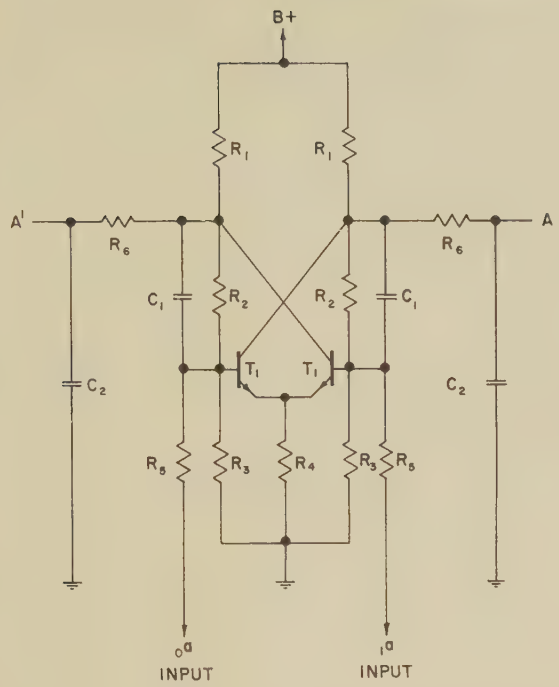


Fig. 5—Transistor flip-flop circuit for low-frequency operation. $R_1=15$ k, $R_2=150$ k, $R_3=56$ k, $R_4=1.5$ k, $R_5=3.9$ k, R_6 depends on clock frequency and load, $C_1=68$ $\mu\mu$fd, C_2 depends on load, T_1 is a Texas Inst. Type 202 NPN.

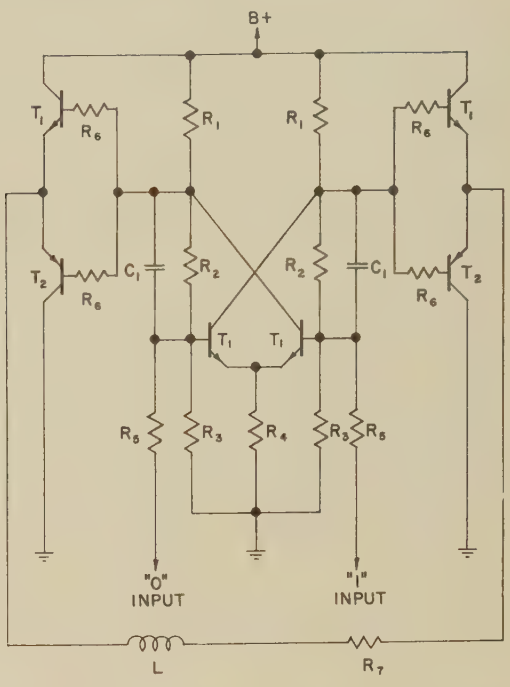


Fig. 6—Transistor "write" Amplifier. $R_1=15$ k, $R_2=150$ k, $R_3=56$ k, $R_4=1.5$ k, $R_5=3.9$ k, $R_6=2.4$ k, R_7 depends upon required dc current, $C_1=68$ $\mu\mu$fd, $L=$inductance of magnetic head, T_1 is a Texas Inst. Type 202 NPN, T_2 is a Texas Inst. Type 301 PNP.

As can be seen from the diagram, the write circuit is essentially a standard flip-flop circuit with the output resistor-capacitor network removed and a recording head connected between the emitter circuits of the output transistors. The availability of *n-p-n* and *p-n-p* transistors allows the use of a coil in the magnetic recording element that does not have a center tap. This is, of course, an advantage where space is a problem, because it enables twice as many ampere turns per given writing current and allowable coil space. The resistor in series with write head is a current limiting resistor.

The additional components required by a computer using this circuitry are a blocking oscillator and a "read" amplifier. These will not be discussed in this paper.

Transistor Differential Analyzer

A transistor digital differential analyzer is being built at the present time which utilizes the circuitry discussed in this paper.[4] The computer was designed to use only five different circuits. These circuits are listed below.

1. Transistor flip-flop circuit.
2. Diode and-or gating circuit.
3. Transistor blocking oscillator to provide the clock pulse used in the computer.
4. Transistor write amplifier for recording on the magnetic disc.
5. Transistor read amplifier for receiving and amplifying information recorded on the magnetic disc.

[4] The differential analyzer is under construction at North American Aviation, Inc., Downey, Calif.

The differential analyzer is fairly complex in that it uses approximately 800 transistors and 3,000 germanium diodes. The computer uses no vacuum tubes. Power consumption, excluding the power for the motor of the magnetic memory, is about 15 watts.

It is believed that the machine will be more reliable than a similar computer using vacuum-tube circuitry. An indication of the reliability is given by data taken on an eight-stage binary counter. It should be indicated that the circuitry has also been tested in a much more complex piece of equipment that was designed to record clock pulses on magnetic storage devices and to run tests on magnetic recording equipment. The allowable parameter variation data taken on the eight-stage counter are presented in Table I.

TABLE I

Parameter	Allowable Variation
Supply voltage (normal 15v)	5v to 25v or ±67 per cent
Most critical resistor	+95 per cent −50 per cent
Germanium diode back resistance	Minimum allowable 2k
Transistors	No selection necessary
Maximum diode gate loading per flip-flop circuit output (Using junction transistors having a cutoff of approximately 1 mc	50 kc—300 gates 100kc—100 gates

It is the author's opinion that the circuitry described herein opens the way for a large amount of work in transistor digital computers in that the circuitry is extremely simple and very reliable. At all times during

the development of this circuitry, simplicity and reliability were stressed. In addition, the use of readily available mass-produced components was assumed mandatory.

Conclusions

A few general conclusions are presented below.

1. All germanium diodes are biased in the reverse direction except when the clock pulse is present. (No transient back resistance problems exist.)
2. The back resistance of germanium diodes used in the computer need only be approximately $2N\ R_F$ or greater, where N is the number of diodes connected to the and gate resistor and R_F is the maximum forward resistance of the type diode used under equipment conditions. (Diode back resistance may drop to a few k-ohms before the computer will fail.)
3. Diode forward current is very low. (For the machine mentioned in the paper, peak diode current is 1.0 ma and maximum average current is 0.050 ma.)
4. A large number of gating circuits can be connected to a given flip-flop circuit output capacitor.
5. Maximum average collector current per transistor is very low.
6. Maximum average transistor collector dissipation is also extremely low.
7. Fast transient response is not required of the capacitor charging junction transistors.
8. No high pulse currents are required to flow in the transistors.
9. The circuitry is not critical with respect to transistor characteristics. (In the flip-flop circuit used, 100 per cent of the transistors received that met manufacturer's specifications worked properly).
10. All logical clock gating resistors are identical.
11. The amplitude, shape, or duration of the clock pulse is not critical.
12. The logical circuitry of the computer is dc coupled. The only ac-coupled portions of the computer are the read amplifiers and the blocking oscillators.

A High-Speed Permanent Storage Device*

JOSEPH M. WIER†

Summary—**This paper describes a device useful for the permanent storage of digital information which ordinarily is not to be altered once it is stored. The device utilizes a large magnetic-core matrix switch, of a type described by Rajchman, in conjunction with a storage system used with the Bell Computer, Model VI, to obtain permanent storage capacities up to about a million bits. The information is stored by suitably lacing a set of drive leads from the output of the magnetic switch through an array of magnetic cores. This device is characterized by low-access time, large-operating tolerances, and a relatively small number of magnetic cores.**

Introduction

IT IS OFTEN desirable to store large quantities of information permanently within a digital computer. All computers have some such storage embodied in the manner in which the circuits are wired originally. This report deals with a storage device utilizing magnetic cores to achieve fairly large amounts of information storage with a relatively moderate amount of circuitry.

Some of the more useful material which might be stored in this way is that which is repeatedly used by a computer such as library sub-routines, important constants, and function tables. For example, the storage of sub-routines alone saves considerably in the amount of information which must pass through the input devices. Further, if the access time to this material is short enough, much time can also be saved in the actual running of problems.

Papers by King, Brown and Ridenour,[1] and Ryan[2] have previously described a way of using a flying-spot scanner in conjunction with photographic or other type slides to achieve storage of this type. The magnetic-storage device, discussed in the present paper, is a combination of a magnetic switch proposed by Rajchman[3] and a storage system used with the Bell Computer, Model VI.[4]

A number of problems result from using this combination. These problems have been analyzed and a number of tests on small-storage systems have been made which demonstrate the workability of the method.

In the interests of economy the term "permanent storage device" will be abbreviated to PSD in the following material.

* Original manuscript received June 1, 1954; revised manuscript received December 13, 1954. This work has been supported by the U. S. Office of Naval Research.

† Digital Computer Lab., Univ. of Illinois, Urbana, Ill.

[1] W. K. King, W. B. Brown, and L. N. Ridenour, "Photographic techniques of information storage," Proc. I.R.E., vol. 41, pp. 1421–1428; October, 1953.

[2] R. D. Ryan, "A permanent high-speed store for use with digital computers," *Trans. I.R.E.*, vol. EC-3, pp. 2–5; September, 1954.

[3] J. A. Rajchman, "A myriabit magnetic-core matrix memory," Proc. I.R.E., vol. 41, pp. 1407–1421; October, 1953.

[4] E. G. Andrews, "The Bell Computer, Model VI," Proc. of Second Symposium on Large Scale Digital Calculating Machinery, Harvard Univ. Press, Cambridge, Mass.; 1951.

Logical Design of a Parallel Permanent Storage Device

Fig. 1 shows the logical design of a parallel PSD. The device shown stores eight words of m bits each. Each one of the output positions corresponds to one of the binary positions of the m digit word. The information is stored in the manner of wiring of the multiple "OR" circuits. Thus, considering word number 1 in the figure, it is seen that there is a connection from word line number 1 to the output "OR" circuits in positions 1, and m and no connection to position 2. As a result, when word line 1 is activated, the output from the "OR" circuits in positions 1 and m will be activated, indicating a "1" in those positions, and a "0" in position 2. The other word lines are similarly arranged so that there is a connection to the "OR" circuits at those positions where it is desired to store a "1" and no connection at those positions where it is desired to store a "0." The number of circuits required is equal to that of binary "1's" to be stored. It is evident that for very large storage capacities the usual triode or diode "OR" circuits are prohibitively expensive because so many are required.

A Parallel Permanent Storage Device Using Magnetic Cores

The Bell Computer, Model VI, uses large magnetic cores in a way which allows the machine to be programmed by threading wires through them.[4] The cores are selectively linked or not linked by the program wires depending upon the orders to be stored. In operation, relays select the program wire circuits sequentially and apply signals to them. Thus signals appear on the secondary windings of all of the cores which are linked by the activated wire and no signals appear on the remaining secondaries. This system has the same logical behavior as that indicated in Fig. 1.

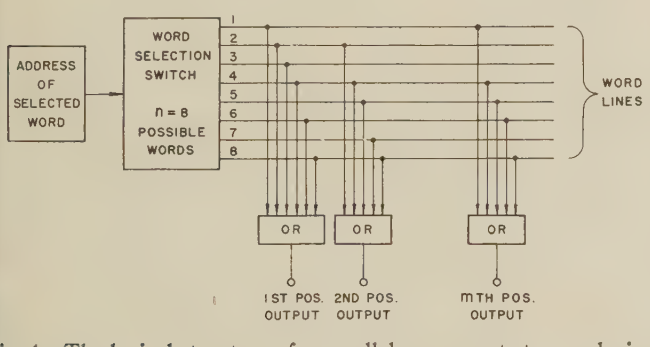


Fig. 1—The logical structure of a parallel permanent storage device. The logical arrangement for a PSD of eight words, each of m binary digits, is illustrated.

Since the relay selection system is relatively slow, it is desirable for many applications to be able to operate at much higher speeds. A vacuum tube equivalent of the relay drivers could be built, but this system would involve a prohibitively large number of tubes for a large storage capacity. In addition, a large impedance mismatch generally occurs. For these reasons it was decided to try a magnetic matrix switch driver. A dc-biased matrix switch has been described by Rajchman.[3] This switch contains one magnetic core per possible output. A rectangular array of cores made of square-loop magnetic materials is biased with a single dc winding such that all cores are biased into their "negative" saturation regions. Then each row and each column are linked by a winding which may be driven so as to cause a magnetomotive force which opposes the bias magnetomotive force. This opposing force is of such a magnitude as to require that both the column and row windings through a core be activated to cause the core to be unsaturated and driven to the positive saturation region. Thus a given core of the array may be selected by driving one row and one column winding which intersect at the selected core. The output winding of each of the magnetic switch cores passes through, or does not pass through, each one of a further set of magnetic cores in accordance with the information to be stored.

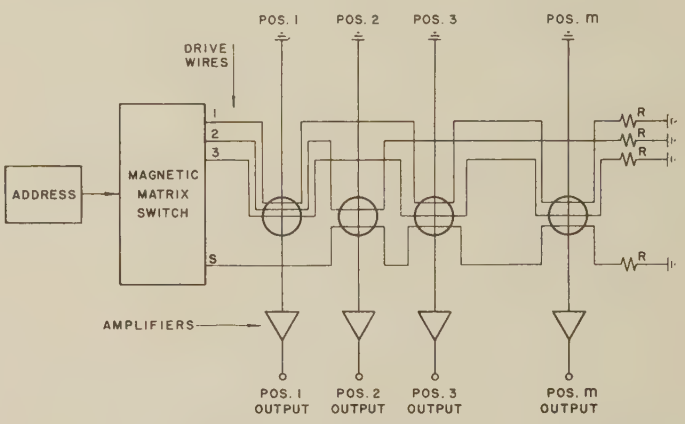


Fig. 2—A magnetic-core permanent storage device. The general layout of a magnetic-core PSD is shown.

Fig. 2 illustrates an elementary PSD constructed in the manner just described. In order to bring a given word of stored information out of the storage array, the following steps are taken. First, assume that all of the cores to the right are set to their negative remanent points. Then the address of the word to be selected is decoded by the magnetic switch and the proper drive wire is activated. The current carried by this wire forces all of the linked cores in the right-hand array to their positive remanent points. During this operation, a signal appears at the input to the amplifiers at each digit position in which a "1" is stored. These signals, or their absence, are interpreted as the stored information at the output terminals. For instance, if word 1 were selected, the output information would be "1" at binary position 1, "0" at position 2, "1" at position 3, and "1" at position n.

Special Problems Associated with This Magnetic-Core Permanent Storage Device

The magnetic switch driver makes it necessary to consider some problems which are not present in a device of the Bell type. Since a magnetic switch does not

actually physically break the drive wires, the drive-wire circuits are always present at least as single-turn loops loaded with their terminating resistors. This causes all of the undriven drive wires to act as transformer secondaries on the driven cores in the storage array when any drive wire is activated by one of the cores in the magnetic switch. These secondaries have two results: coupling through them back to the undriven cores causes the signals at the outputs of these undriven cores to be different from zero, and the secondary currents react back on the primary drive circuits, making more difficult the turning over of the linked cores.

Fig. 3 may be used in considering the first of these two difficulties. Let it be assumed that it is desired to select word number 1. Then the drive wire which selects word 1 will be activated by selecting the upper right-hand core in the matrix switch. The selected line links the cores in binary positions 2 and 3. Then, when the cores in these two positions are driven out of the saturation region, where they usually reside due to the dc bias winding, voltages are induced in all of the selection lines linking the driven cores. As all of the remaining lines pass through at least one of the two selected cores, voltages are induced in lines 2, 3, and 4. These voltages are in such a direction as to cause current to flow in a direction opposite to that in the selected line so these currents cause the unselected cores to be moved farther back into the negative saturation region. Thus if a large positive signal is obtained from the selected cores, a small signal of opposite polarity appears at the output of each of the unselected cores. As a result, the secondary coupling is of benefit in improving the difference between a selected signal and an unselected one.

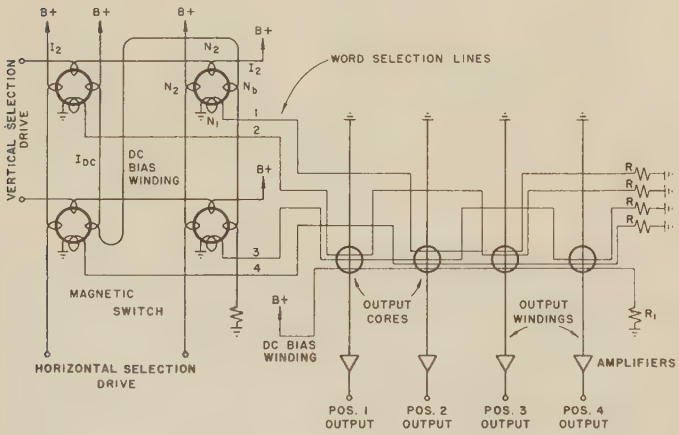


Fig. 3—An elementary four-word magnetic-core PSD. A schematic of the electrical arrangement of a magnetic-core PSD containing four words of four binary digits each shows the manner in which this type of storage system is connected.

The second difficulty, that of the reaction of these secondary currents back on the primary-drive circuit, is a bit more troublesome. Since each core is linked by many drive circuits and each of these has a terminating resistor, R, in it, the effective impedance of the secondary as viewed from the primary-drive circuit becomes proportionately smaller as the number of secondaries increases. This means that the net flux changes in the selected output cores are decreased as more and more bits are stored per core. Thus the selected output core delivers less output signal with larger storage capacities. In fact, the ultimate practical limit to the storage capacity per core is governed by this condition.

There are two storage patterns which will cause difficulty. One of these is that existing with many secondaries linking all of the cores in the storage array. The other pattern is shown in Fig. 4. With the latter pattern it is possible for the coupling from the drive wire m to the nth output through storage core n to actually be reversed in sign. This condition must be avoided at all costs. The state of the storage array in which all storage cores are linked by all drive wires is also annoying, and although it cannot cause a reversal of the output, it may still reduce the output signal to an unusable low value when a large number of secondaries are present.

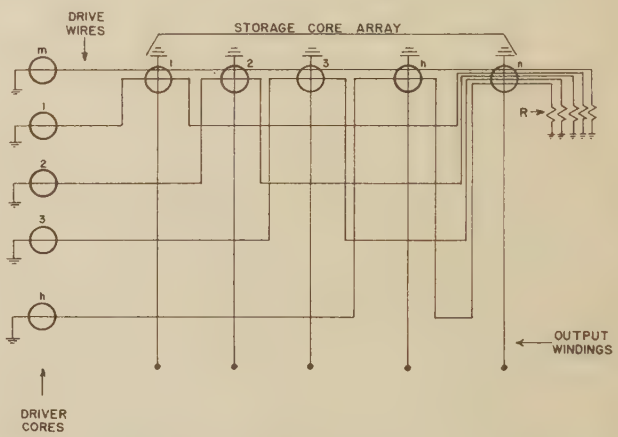


Fig. 4—An undesirable storage pattern for the permanent storage device. A condition of information storage which can result in the most degradation of an output signal is illustrated.

To analyze these difficulties, assume that the peak output voltage from a storage core, when it is turned over, is proportional to the net drive current. Then, at that peak, we may define the peak core-voltage drop as e_c and the peak current as i_c. Since these are assumed linear functions of each other, define an impedance, Z_s, as

$$Z_s = \frac{e_c}{i_c}. \tag{1}$$

Also let the coupling be assumed good enough so that the voltage, e_s, induced in every secondary is identical to the drop in the primary-drive wire. First, treat the case illustrated in Fig. 4. The current, i_s, resulting in each secondary when drive wire m is activated is

$$i_s = -\frac{(e_s + be_s)}{R} = -\frac{(1+b)e_s}{R}, \tag{2}$$

where be_s is the inductive voltage drop across core n.

Now, if the total number of undriven secondaries exceeds $(n-1)$, each one of the undriven drive wires may actually be p such wires in parallel. This has the effect of putting p terminating resistors, R, in parallel so that for the undriven drive wires, R in (2) may be replaced by R/p. Making this substitution, (2) becomes

$$i_s = -\frac{(1+b)e_s p}{R}. \tag{3}$$

As a result of the assumption given by (1), the net current in the nth core will be bi_m so for that core

$$bi_m = i_m + (n-1)i_s, \tag{4}$$

where i_m is the current in the driven wire, m. From (3) and (4)

$$i_m(1-b) = \frac{(n-1)(1+b)e_s p}{R}. \tag{5}$$

When the loss of signal in passing through any but the nth core is not very large, it may be written that very nearly

$$\frac{e_s}{i_m} = Z_s. \tag{6}$$

Then (5) becomes

$$R = \frac{Z_s(n-1)(1+b)p}{(1-b)}. \tag{7}$$

Let the number of words to be stored on the n core array be c and let the length of these words be r bits. Then

$$r = n, \tag{8}$$

and

$$c = 1 + p(r-1). \tag{9}$$

From (8) and (9) we may alter (7) to

$$R = \frac{Z_s(r-1)(1+b)(c-1)}{(1-b)(r-1)} = \frac{Z_s(1+b)(c-1)}{(1-b)}. \tag{10}$$

Thus R, for a given value of signal degradation factor, b, is independent of the word length, but is directly proportional to one less than the number of drive wires.

When all of the drive wires link all of the cores, a similar analysis may be made. With c drive wires and r cores, the current in a given undriven drive wire with terminating resistor, R, is,

$$i_s = \frac{e_s r}{R}. \tag{11}$$

The net current linking a storage array core is bi_m for a signal degradation factor of b. Then

$$bi_m = i_m - \frac{re_s(c-1)}{R}. \tag{12}$$

Since

$$e_s = be_m, \tag{13}$$

where e_m is the normal unloaded peak value of the induced voltage, and

$$\frac{e_m}{i_m} = Z_s, \tag{14}$$

the following results when these are placed in (12):

$$R = \frac{r(c-1)bZ_s}{(1-b)}. \tag{15}$$

For given values for Z_s, r, R, and $(c-1)$ the degradation factor, b, may be compared in the two cases. From (10)

$$b = \frac{R - Z_s(c-1)}{R + Z_s(c-1)}. \tag{16}$$

From this it is evident that b may become 0 or even go negative which would result in an error in reading being indicated in position n. Thus the size of c is restricted for a given R and so the amount of information stored in the r core array is limited by the allowable degradation in the output signal in this case. Since c may be raised at the expense of increasing R, we may get more information stored per core, but a correspondingly larger amount of driving power will be required since the current demands for turning over the cores will not decrease. From (15) the value found for b in the other case when all cores are linked by all drive wires gives

$$b = \frac{R}{R + r(c-1)Z_s}. \tag{17}$$

This quantity will never go negative or even go to zero for r and c finite, but it may easily become very small. Again the solution is to make R large, again at the expense of increasing the driving power.

To compare the two in their limiting effect on b, assume that it is desired to make b, R, and r equal in the two cases with the same Z_s. Then the most undesirable case to be considered is the one yielding the smaller c. From (16),

$$c_1 = 1 + \frac{R(1-b)}{Z_s(1+b)}, \tag{18}$$

and from (17)

$$c_2 = 1 + \frac{R(1-b)}{brZ_s}. \tag{19}$$

These differ only in a portion of the second term. Thus it is convenient to compare $1/(1+b)$ with $1/(br)$. Since it is desirable that b be a reasonable fraction of 1, and since r will be one word length,

$$\frac{1}{(1+b)} = \frac{1}{br}, \tag{20}$$

so the second case, that of the common linkage of all cores, is the case which will restrict the storage capacity per storage array core. Thus, using (19), it is seen that

for large storage capacities per core, R should be large and b, r, and Z_s should be small. As R is limited by the amount of pulse power available to drive the system and the required turnover current of the core, and b and r are restricted by the allowable attenuation from one storage core to another and the word size, respectively, only Z_s may be controlled. Thus cores should be used which have small ratios of voltage drop to driving current. This implies toroids with a large ratio of diameter to cross section.

Actually this is rather pessimistic for, in any practical storage system, this pattern never would be even approximated. However, these at least give bounds on c which will definitely produce a satisfactory result.

The above facts do not limit the actual storage capacity, but they do dictate that only c bits of information may be stored per core in the storage array. In order to increase the capacity without increasing the number of cores in the selection switch, each drive wire may link or not link kr cores where k is an integer determined by the desired storage capacity. Each of the r output windings links one of the r cores in each of the k sets of cores in the storage array. Then, when a given word is to be read out on one of the drive wires, all but one of the k sets of r cores are saturated, and the information read is merely that stored on the unsaturated r cores of the array.

Tests were conducted with a 10-binary position model and the above design criteria and available materials. It was found that, with a driving pulse power of 50 watts and using standard square-loop ferrite cores, it is possible to store over 100 bits per core without reducing b to less than 0.25. Since no very critical analog property of the cores is used, the device is very insensitive to reasonable core variations. Since only the switching properties are used, very high turnover speeds may be achieved merely by increasing the driving currents. In test experiments, turnover times of less than 2 microseconds have been used with steel cores, and times of less than 1 microsecond are easily obtained using ferrite cores.

Applications

It has become general practice to collect a fairly extensive library of sub-routines with every large-scale digital computer. These are used in the preparation of other programs and, as such, each of these sub-routines passes through the input devices many times. Thus considerable time may be saved in program preparation if this material is available internally to the machine, even if this material is used only as a library from which to extract sub-routines to be placed in the main program after this program has been inserted into the computer. A further saving may be made which will markedly decrease the running time of many problems. By utilizing the short access time of this stored material, the machine may be controlled directly from the PSD, time being saved in that no transfer to the main memory is required and, further, in that it is usually possible to make the access time to the permanently stored programs less than that to the material stored in the main memory.

A more fundamental application of such a storage system has been suggested by Wilkes and Stringer.[5] By constructing circuitry to do the individual steps of an order and using a stored program to sequence through these steps in any arbitrary order, very complex and elegant order codes may be constructed without resorting to correspondingly complicated circuitry. Further, the alteration of the order code then is much simpler, involving a change in the stored information defining a given order or orders.

Conclusion

The magnetic-core PSD possesses the following desirable properties. It has an access time of the order of 1 to 5 microseconds, including the setting up of the selection system, high reliability due to the noncritical use of the magnetic cores, fairly low cost, a purely digital addressing system, a reasonable storage capacity limit of perhaps a million bits, and a storage-packing density which may be on the order of 50,000 bits per square foot of storage array.

The principal disadvantage is that of inserting or altering the information. Since, in general, this process will occur but once, this is not too serious for reasonable capacity systems.

Because of the above properties it is felt that this PSD is capable of providing permanent electronic storage capacity at a reasonable cost and with sufficient reliability, capacity, and speed for many digital computer applications.

[5] M. F. Wilkes and J. B. Stringer, "Microprogramming and the design of the control circuits in an electronic digital computer," *Proc. Cambridge Phil. Soc.*, vol. 49, pt. 2, pp. 230–238; 1953.

Correction

G. R. Partridge, author of the paper, "A Transistorized Pulse Code Modulator," which appeared on pages 7–12 of the December, 1954 issue of the Transactions, Electronic Computers, has called attention to the following omission.

The quantizing system described in the first part of the paper was disclosed in United States Patent 2,612,550 (September, 1952) issued to Mr. G. T. Jacobi of the General Electric Company. The author regrets that this information was unknown to him.

Control Features of a Magnetic-Drum Telephone Office*

W. A. MALTHANER† AND H. E. VAUGHAN†

Summary—Several functional arrangements useful in conjunction with a parallel magnetic-drum memory are described with general reference to their application in an experimental telephone-switching system. The functions included are detection and registration of input information, counting, timing, transfer of information from one drum location to another, and translation of information from one form to another.

Introduction

A GENERAL description of an experimental automatic telephone switching system using magnetic-drum memory has been presented.[1] Programming and circuitry methods used for the various functions of the system are presented here to those design engineers who are interested in such details. Many of the functions performed by the control section of this system are similar to those in a digital computer. Among these functions are counting, timing, translating information from one form to another, storing, testing, selecting, marking and comparing. Several combinations of these functions are used in each circuit unit.

Five representative circuit units are described in the following pages. Many of the specific details used in the system have been omitted in an attempt to simplify the description of the generalized functions.

Review of the System

Functional Arrangement

Before proceeding to a treatment of the circuit units a brief review of the whole system is given in the following paragraphs as a means of orientation.

The DIAD (Drum Information Assembler and Dispatcher) telephone switching system could be represented most simply by a hypothetical two-block diagram. The switching network, which is the maze of channels through which the conversational paths between subscribers are established, is represented by one block. The control section, which processes information generated by subscribers for the control of these paths, is represented by the other block. The circuits in each of these blocks function with speed sufficient to permit operation of the switching system on a one-at-a-time basis. However, in the control section many different functions, each on a one-at-a-time basis, may be performed simultaneously. The high speed necessary for this type of operation is facilitated by the use of electronic equipment.

General Operation and Synchronizing

A capacitive scanner is used as a time-division connector from subscribers' lines to the magnetic drum and its associated circuits. The drum provides for the storage of both temporary and "permanent" information. One section of the drum memory is associated with subscribers' lines and the other section with the output side of the switching network, that is, with the trunks. On each call complete information is finally assembled in the trunk section of the drum memory and retained there for the duration of the call. A built-in program directs the processing of information. Programming is controlled by a series of call progress marks, one of which is written in the drum slot each time a new stage in the program is reached. Information dispatched from the trunk drum directs the operation of the switching network and also the signaling to other offices.

Each group of information, which forms an item of control data, is entered on the drum or read from it in parallel channels rather than serially in time from one channel.

Each subscriber is assigned a fixed plate on a line scanner, and the line drum slot is indexed by this plate. The scanner inspects each line plate 60 times a second with a period of 16 microseconds for each inspection of each plate. All of the information recorded in the associated slot on the drum is available for reading and alteration simultaneously during each inspection period. Alteration of the information in the cells of a drum slot made while these cells are still under the same heads just used for reading is called "single-pass" operation.[2] For this purpose each scanning period is divided into a read period of 2 microseconds, a write period of 3 microseconds and an eleven microsecond idle period. This division is accomplished by reading all cells in one drum slot under control of a read-sync pulse and writing in these cells under control of a write-sync pulse. When it is necessary to extend the duration of a pulse from the reading time to the writing time, a toggle circuit is operated. The toggle is reset at the end of the write-sync pulse by a reset-sync pulse. Other basic elements used in the control of circuits are germanium-diode gates and matrixes, vacuum tube multivibrators, cathode followers and inverters.

Coding and Checking

Each decimal digit of data in the control section is nominally coded so that marks are present in exactly two of five parallel channels assigned to the digit. On every operation in which information is transferred from the drum to a register, the information digits are checked by a check circuit about 0.8 microsecond after the start of the read-sync pulse. If the data checked

* Original manuscript received November 22, 1954.
† Bell Telephone Labs., Murray Hill, N. J.
[1] W. A. Malthaner and H. E. Vaughan, "An automatic telephone system employing magnetic drum memory," PROC. I.R.E., vol. 41, pp. 1341–1347; October, 1953.

[2] J. H. McGuigan, "Combined reading and writing on a magnetic drum," PROC. I.R.E., vol. 41, pp. 1438–1444; October, 1953.

conforms to the code, control functions associated with the register proceed. If an error is detected, a trouble condition is recorded, and the registers are cleared so that the circuit may serve some other request. The information which did not check is held on the drum so that it can be inspected in the maintenance process. In a commercial system a trouble report would be printed and, to avoid service interruption, a second trial would be made immediately.

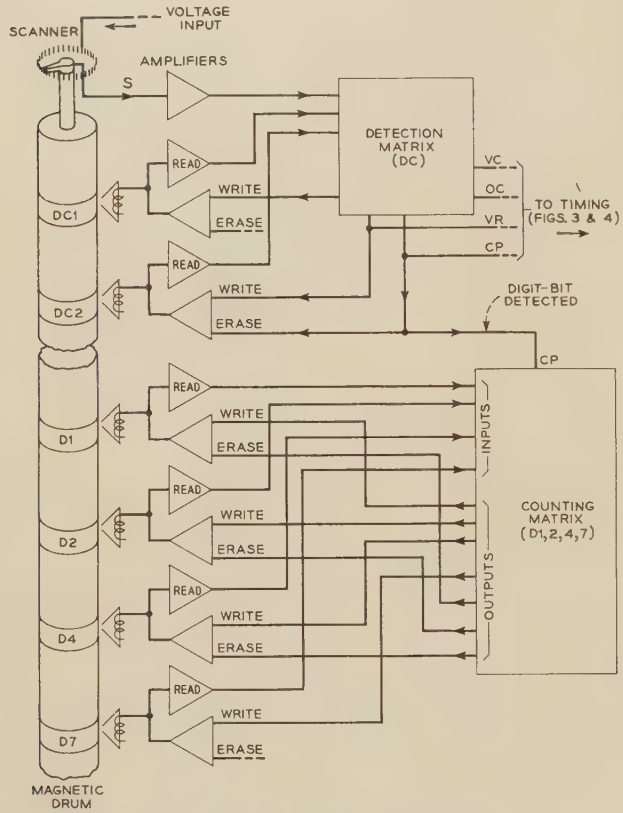


Fig. 1—Digit detection and counting.

Boolean algebra was used in the design of a large part of the circuitry. The logical operation of some of the circuits is summarized in truth tables. The combination of a block diagram and a truth table is often sufficient to convey the information concerning operation of a circuit to those familiar with computing units and thereby save reading of detailed text.

With this system background in mind, the following sections present an operational description of the five characteristic circuit units.

Pulse Detection and Registration

One of the basic problems in automatic telephone switching is the detection and registration of the information generated by switches in the subsets of the subscribers. In this system the information appears as voltage changes on a conductor leading to the telephone subset. The capacitive scanner is used to connect each such information source to the information assembling circuits of a magnetic drum on a time-division basis. Each information source applies voltage via its individual input conductor to a fixed plate of the scanner at the start of a transmission operation and generates digital information signals by interrupting the voltage a number of times equal to the digit. Successive digits on a conductor are separated by the continuous application of voltage for an interval somewhat longer than that occurring between the interruptions representing a single digit. The minimum duration of a voltage application or interruption must, of course, be long enough to permit its detection by the scanner at least once.

The circuits, shown in Fig. 1, are time-shared by 1,000 lines. Each line has access to these circuits for only about 5 microseconds out of each 16 microsecond time-slot on each revolution of the scanner and drum. Thus, this circuit may be thought of as a computer unit capable of handling 1,000 simultaneous problems on a time-division basis. The logical operations are best understood by considering a particular time slot and the functions occurring in this slot on successive revolutions.

The outputs of the line scanner and of two "data control" drum channels are required to recognize and record the significance of a sequence of changes in line conditions. A typical sequence of conditions on the scanner and these two drum channels for one of the 1,000 input lines is shown in Fig. 2. These conditions appear on the circuit outputs only once per revolution in their associated time slot. These pulse outputs are regenerated at their point of entry into this circuit by toggle circuits. The function of these toggles is to extend the 2 microsecond "read" pulse until the end of the "write" pulse. Each toggle supplies two polarities to the inputs of the diode Detection Matrix (DC). The (DC) matrix provides outputs for altering the magnetic records in the DC1 and DC2 channels as well as outputs to other counting and timing circuits, as summarized in Table I on the opposite page.

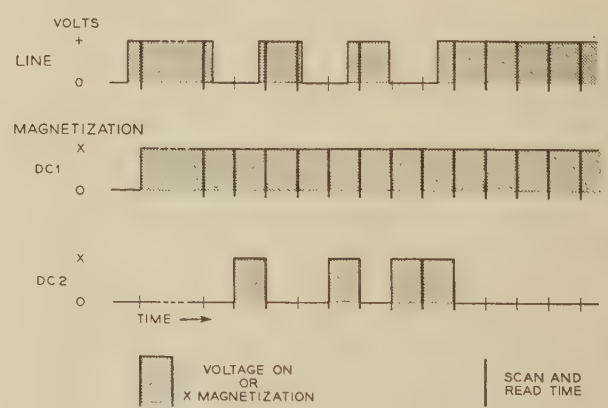


Fig. 2—Typical sequence of conditions for one input-line.

Initially there is no output signal from the scanner and there are no magnetic marks in the DC1 and DC2 cells. On the first drum revolution after a signal voltage appears on the line plate, the output of the scanner, S, causes a mark to be written in the DC1 cell as the first output of the (DC) matrix. On the next revolution of the drum a Voltage-Continued, VC, pulse produced by combining the outputs of the S and DC1 channels in

TABLE I

	Inputs			Outputs					Significance
	S	Read DC1	Read DC2	Write DC1	Write DC2	CP Erase DC2	VC	OC	
a									Idle condition
b	1			1					Initial voltage detected
c	1	1					1		Voltage continued
d		1			1				Voltage removal detected
e		1	1					1	No-voltage continued
f	1	1	1			1			Digit-bit detected. Return to condition on row C

1 = Presence of signal.
Blank = Absence of signal

the (DC) matrix is generated. This signal starts the action of timing circuits to test for a trouble condition of voltage permanently on the line and for interdigital intervals between trains of data pulses. These timing actions will be described later.

When the signal voltage is interrupted the scanner output is zero. This output is combined with the output from the DC1 channel to produce an output from the (DC) matrix which is registered in the DC2 cell. Subsequent reappearance of voltage is detected by the scanner. This scanner output is combined with the outputs of DC1 and DC2 to produce the Complete Pulse, CP, output of the (DC) matrix. The CP output pulse causes the erasure of the mark in the DC2 cell and enables the D-matrix. As shown in Fig. 2, the record in the DC2 channel is an inverted and time-quantized representation of the line condition after the initial closure of voltage to the line. Thus, changes in the condition of the line are detected in the (DC) matrix by comparing the output of the DC2 channel with the scanner output. Another output of the (DC) matrix, OC, is produced by a continued "no voltage" condition after an initial application of voltage. The absence of a signal on the scanner output at a time when there are marks in both the DC1 and DC2 cells produces this Zero-Continued, OC, output which initiates a timing cycle.

The functions just described are: the production of a memory record indicative of the present significance of a sequence of time-spaced signals; the detection of any change indicated by the latest signal; and the alteration of the memory record in accordance with a detected change.

As mentioned above, at the completion of each data pulse the CP output of the (DC) matrix is applied to the matrix which controls the D-channels. These pulses generated in response to each pulse of a train of data pulses are counted so that the digit is accumulated in the group of four D1 to D7 cells. Those cells which are to be marked and those to be erased depend upon the pulse count already stored when a CP pulse occurs.

The code used here is a modified binary-decimal one in which not more than two of the four code elements are energized to represent any decimal value. The numbers 1, 2, 4 and 7 are assigned to the code element places. The decimal value of a digit is then the same as the number of the energized code element or is the sum of the two energized code-element numbers. The only exception is the decimal digit 0, which is represented by elements 4 and 7. At a later stage this code is modified by adding a fifth code element, numbered 0, energized as required to provide the uniform 2-out-of-5 code shown in Table II below. This is the checkable code previously discussed. Thus, this group of circuits perform the logical functions of counting pulses (on the CP lead) and coding the current total count into a magnetic record.

TABLE II

Digit Value	2-Out-of-5 Code*				
	D7	D4	D2	D1	DO
1				1	1
2			1		1
3			1	1	
4		1			1
5		1		1	
6		1	1		
7	1				1
8	1			1	
9	1		1		
0(10)	1	1			

* 1 = presence of marks or signal.

Timing and Lateral Transfer

Trains of pulses representing digits are separated by continuous application of voltage for an interval somewhat greater than the application of voltage between digit pulses. One method of detecting such a longer interval of continuously applied voltage is to measure the duration of each such application and to compare the measured interval with a predetermined interval.

In this particular case the predetermined interval is seven revolutions of the drum.

At the end of the train of data pulses constituting a single digit, the VC output of the (DC) matrix is present for several drum revolutions. During this interval a timing circuit, Fig. 3, employing three "fine-timing"

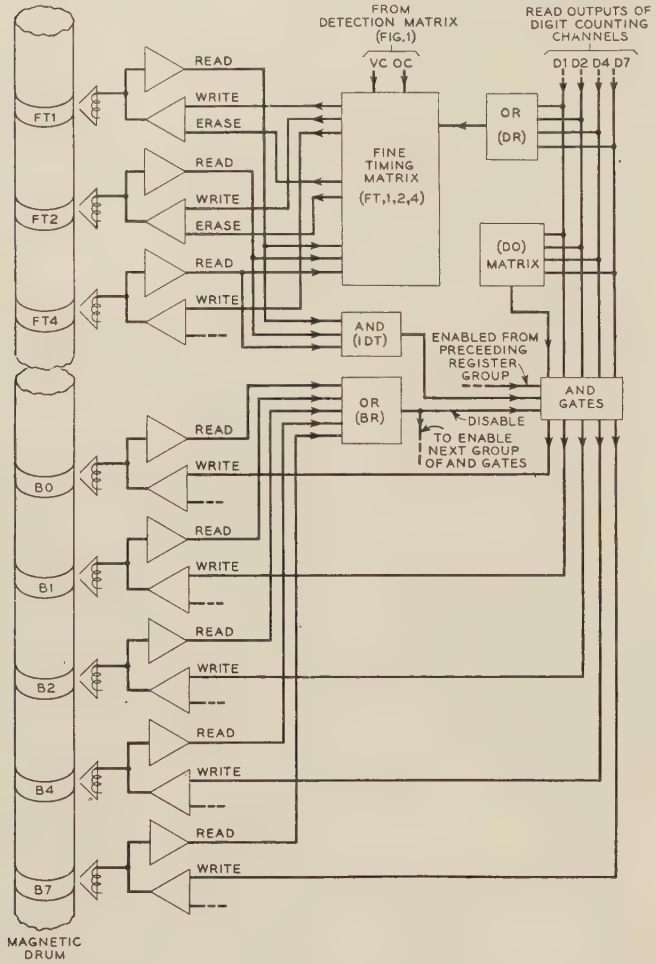


Fig. 3—Interdigital timing and digital transfer.

channels on the drum, is enabled to count seven revolutions of the drum on a binary scale as an indication that an interdigital interval has elapsed. If a "no voltage" condition occurs before the completion of this timing cycle, the timing circuit is reset. The presence of some registration in the D-cells is indicated by a pulse on the output of the D-digit registered (DR) gate. The simultaneous occurrence of a DR and VC pulse produces a pulse, which is combined with the outputs of the FT1, FT2 and FT4 fine-timing channels of the drum in a matrix, to control the writing and erasing of marks in these channels. When these timing channels indicate that the VC condition has persisted for seven revolutions of the drum an inter-digit-time pulse, IDT, is produced at the output of the (IDT) gate. This pulse causes the digit accumulated in the D-cells to be shifted to other cells in the same slot, at the same time clears the D-cells, and when necessary, causes the recording of a call progress mark. Erasure of all accumulated timing marks takes place when the digit is removed from the D-channels to other storage. Erasure of all timing marks also takes place immediately upon premature interruption of the timing cycle. The function performed here is that of timing the duration of a condition by counting elapsed-time intervals into a binary magnetic record.

Furthermore, when a digit is shifted to other cells, the code is amended if necessary to provide a true 2-out-of-5 code by recording a mark in the O cell. This is accomplished by connecting the read outputs of the D-channels to a (DO) diode matrix which performs the "add-check channel" function. An output of the matrix is energized if there is a mark in one and only one of the four D1 to D7 cells.

Groups of cells may be provided for the registration of as many digits as desired. These groups are used in a preassigned order, the registration present in one group directing the master-enabling pulse to the next idle group.

The master-enabling pulse is transmitted to all the writing gates associated with the cells to which the registration is to be shifted upon the occurrence of an IDT pulse, provided there is no registration already in those cells. This master pulse is combined with the outputs of the D-cells and with the DO output of the (DO) matrix to cause a repetition in the selected group of cells of the record in the D-cells modified to provide a 2-out-of-5 code. These processes are repeated until all wanted information is accumulated. Thus, the above circuits perform the functions of lateral transfer of data to a selected new location in the same drum slot and its conversion during transfer to a checkable form.

Coarse Timing

Timing of conditions which exist for periods of time that are long as compared to a revolution of the drum and that need not be measured with much accuracy is accomplished as follows. Every slot where such a condition may exist is examined at regular intervals. In the circuit shown in Fig. 4, when the condition is first detected during such an examination, a mark is recorded in channel CT1. If, at the next examination the condition still exists, this, together with the mark in CT1, shows that the condition has existed for at least one interval, but for not more than two intervals. This fact is recorded in CT2, and is used to initiate any appropriate action. If, before the second examination the condition is removed, the mark in CT1 is immediately erased. By this means the appropriate action referred to is initiated when the condition exists for 1.5 ± 0.5 intervals.

The circuits at the top of Fig. 4 show in a little more detail how, at each periodic examining time, an enablement to control the writing of these two marks is produced. Each enablement must have a duration of exactly one revolution to insure that in each slot only a CT1 or a CT2 mark can be written, or, in other words, so that two enablements separated by a suitable time interval will be required for the writing of both marks.

The time interval between enablements is established by basic input pulses having a time-spacing equal to the minimum significant duration of the condition to be timed. A toggle operated by one of these basic pulses permits pulses occurring once per revolution of the drum to operate a binary-counter stage. One revolution pulse operates the binary counter, and the next such pulse resets the counter and indirectly the toggle. Thus, the binary counter produces the one revolution-timing enablement. Two such enablements with different repetition rates are shown in Fig. 4.

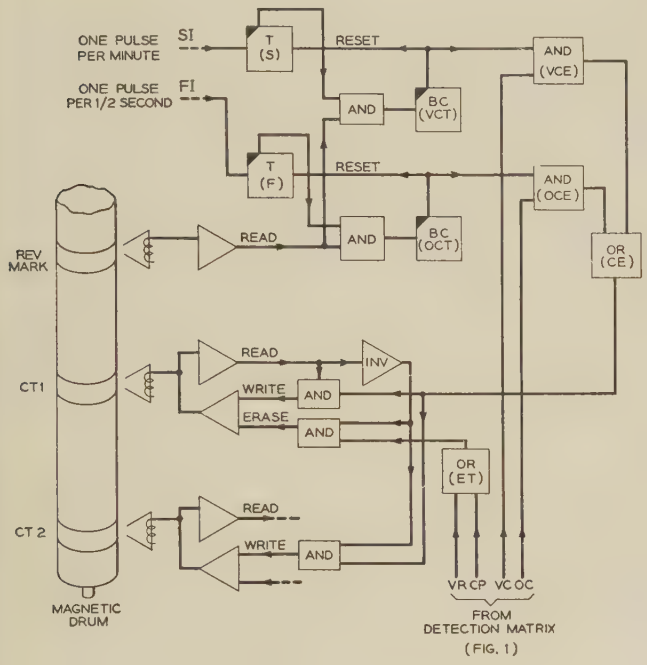


Fig. 4—Coarse timing.

In the telephone system one of these enablements is used to control the timing of one interval on continued presence of voltage on the line, and the other enablement is used to control the timing of a different interval on continued removal of voltage from the line. A mark in CT2, together with a program mark, indicates which particular timing condition has been completed.

The timing cycle just described illustrates one way in which a whole class of time-measuring functions may be economically realized when the accuracy required is less than that obtainable by counting drum revolutions and the intervals are so long as to make the revolution counting method unattractive. This example also shows how the same memory channels may be used in one slot at different times for two timing operations. In addition the same circuit and channels may be used for simultaneously timing the first condition in one group of slots and the second condition in another group of slots.

Drum to Drum Transfer

Another important function performed in the DIAD system is that of transferring information from a group of cells in a slot on a drum to another slot on the same drum or to a slot on another drum in accordance with a particular order. In other cases information received from some external source must be registered at a particular address on a drum. The basic process is the same for all cases and will be described with the aid of Fig. 5.

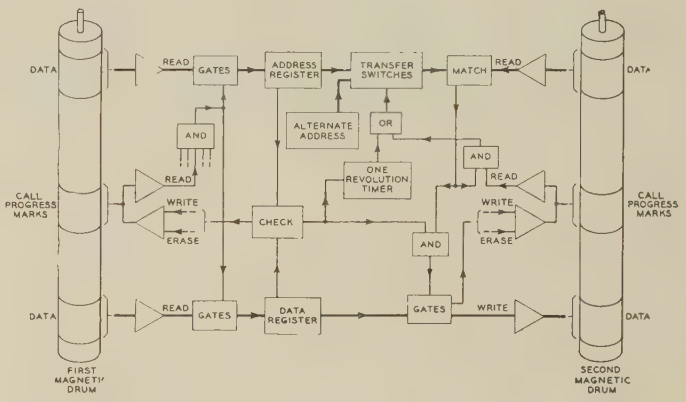


Fig. 5—Drum-to-drum transfer.

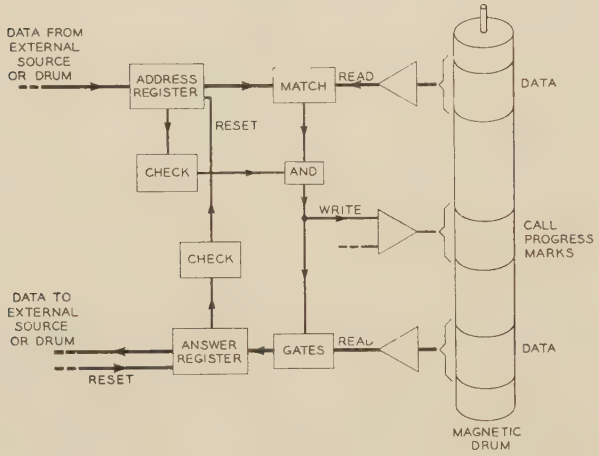
When the information is taken from a slot on the drum, a call-progress mark and other orders are combined in a master diode-logic circuit. The pulse from this circuit is combined with the data pulses in a set of gates so that vacuum tube register toggles are operated in accordance with the data. This registration is checked by a check circuit, and if it conforms to the code, the process of selecting an address on another drum is started. If the data does not conform, a trouble condition is recorded, and the registers are cleared so that the circuit may serve some other request. Part of the data is used as an address, and the remainder is registered on the drum at this address. The address data is applied to one side of a match circuit. Possible addresses, one of which identifies the slot in which the data is to be registered, are read from the drum and applied to the other side of the match circuit. When the address in the register and one from the drum correspond, a match pulse is generated as an indication that the proper slot has been located. Since this pulse controls logic circuits which write information on the drum in this same time slot, it must occur shortly after the start of the read pulse. In this circuit the match pulse occurs about 0.6 microsecond after the read pulse, so that approximately 1 microsecond is available for operation of the logic circuit. In the DIAD system a call progress mark is written at the same time as the registered data. This process demonstrates the advantage of "single-pass" operation.

Occasionally the address sought is in use. If this happens to be the case, an alternate sub-routine is followed. If a match is found and access to the slot denied, due to the presence of an inhibiting call-progress mark, an alternate address to which access will be available is substituted. A match is then made with the substitute address. Alternatively if a match is not found in one revolution of the drum, an alternate address is also substituted. Shortly after a match is made, the register circuits are reset so that they may serve some other case.

These circuits function in one-half drum revolution on the average, and only one problem is handled at a time.

Translation

Another function necessary in most common control systems is that of translation between related sets of data previously recorded in the memory. In the telephone case memory is entered with the directory number of a subscriber to get the equipment number or switch position of a subscriber. In the computer problem



. Fig. 6—Translation.

this might be the case of entering a table with the sine of an angle to find the angle. A block diagram of this process is shown in Fig. 6. The operation is quite similar to the case of transferring information described above. The address is placed in a register, and a match is sought between this registered address and addresses on the drum. When a match is found, a "match" pulse is generated, which is combined in a group of AND gates with the translated number, to produce pulses that operate a set of registers for the translated number. This same "match" pulse controls writing of a call-progress mark in the same time slot. Here again "single-pass" operation on the drum is used to advantage. The holding-time of the circuit in this case is an average of one-half revolution of the drum plus the time necessary to use the translated number and clear the register.

Conclusions

A laboratory model of the DIAD system, which uses various combinations of the functions described above, has been built and has been operating successfully for some time. The continued operation of actual circuits for all the functions demonstrates that such a system is realizable. The maintenance required in this period of continued operation has been quite moderate and has been accomplished in a straightforward manner by laboratory technicians. Circuit arrangements of the type discussed here may be of use not only in future telephone systems but also in many control systems for the accumulation and processing of data.

Acknowledgment

The success of this laboratory model is the result of the united effort of the various men who have built, have tested, and are maintaining the system. In particular, thanks are extended to G. G. Bailey and G. A. Backman, who performed a large part of the work.

Stability of a Method of Smoothing in a Digital Control Computer*

WILLIAM KARUSH†

Summary—**In a certain operation a digital computer was used as an element of a control system to smooth consecutive observational data. The method of smoothing consisted of predicting from past smoothed values and then combining the prediction with the next observation. In this paper an analysis of the stability of this useful method is made, and an explicit formula of the range of the parameters for which the method is stable is derived. Also, the statistical variance of the smoothed variable is calculated.**

Introduction

THE problem which is considered in this paper arose in an operation in which a digital computer was employed as an element of a control system. One of the purposes of the computer was to smooth incoming observational data containing noise. The smoothing procedure used was to predict a value of the variable in question by means of preceding smoothed values, and then to combine this predicted value linearly with the observed value employing weighting coefficients α and $1-\alpha$ $(0<\alpha<1)$. The prediction was based upon a polynomial approximation of degree q; thus the method depends upon two parameters, q and α, fixed for a particular smoothing procedure.

This smoothing method is computationally simple and rapid, iterative in character, and easy to code. It is subject to instability, however, for certain values of the parameters. The purpose here is to derive an explicit formula for the range of stability so that the method may be used with safety. Also considered is the calculation of the statistical variance of the smoothed variable.

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To describe the method more specifically, consider a random variable which is a function of time. Let experimental measurements be made at equally spaced consecutive times $n=1, 2, 3$, etc. to produce a sequence of sample values ξ_1, ξ_2, ξ_3, etc. At time n the n data $\xi_1, \xi_2, \cdots, \xi_n$ have been observed, ξ_n being the latest observation. It is now desired to calculate a "smoothed" value x_n for the "raw" value ξ_n which is to be a function of the observations to date; this calculation is to be carried out before the next observation is used, and then the process is to be repeated with the new observation. The special case of "linear prediction" of the general method treated herein may be described as follows. We suppose that the smoothed data $x_{n-1}, x_{n-2}, \cdots$ are available and the next value x_n is to be calculated. The first step is to predict a value of x_n by linear extrapolation from the two preceding values; denote this value by $L(x_{n-1}, x_{n-2})$:

$$\begin{aligned} L(x_{n-1}, x_{n-2}) &= x_{n-1} + (x_{n-1} - x_{n-2}) \\ &= 2x_{n-1} - x_{n-2}. \end{aligned}$$

The next step is to combine this predicted value with the unsmoothed datum ξ_n using weighting coefficients α and $1-\alpha$, $0<\alpha<1$. The complete iteration formula is therefore

$$x_n = \alpha L(x_{n-1}, x_{n-2}) + (1-\alpha)\xi_n, \qquad 0<\alpha<1.$$

Any convenient initial values for x_1 and x_2 may be taken; for example $x_1=\xi_1$, $x_2=\xi_2$.

The general method treated herein[1] comes about by replacing the first degree prediction $L=2x_{n-1}-x_{n-2}$ by a general q^{th} degree prediction

$$L_q(x_{n-1}, x_{n-2}, \cdots, x_{n-q-1}), \qquad q \geqq 1,$$

L_q being the value at n of the polynomial of degree not exceeding q which assumes the values $x_{n-1}, x_{n-2}, \cdots, x_{n-q-1}$ at the argument values $n-1, n-2, \cdots, n-q-1$. L_q is a certain linear combination of its arguments. The difference equation satisfied by the smoothed values is

$$x_n = \alpha L_q(x_{n-1}, x_{n-2}, \cdots, x_{n-q-1}) + (1-\alpha)\xi_n, \qquad (1)$$
$$0<\alpha<1.$$

Initial values $x_1, x_2, \cdots, x_{q+1}$ may be chosen in any convenient way.

The main question considered here is the *stability* of the smoothing process as a function of α (and q). We regard (1) as a linear difference equation to be solved for x_n in terms of an arbitrary given sequence ξ_n and arbitrary initial values. The principal result is the following:

Let

$$\alpha_{\text{crit}} = \frac{1}{\left(2\cos\dfrac{\pi}{q+1}\right)^{q+1}+1}, \qquad q \geqq 1. \qquad (2)$$

Then the solution of (1) *is stable for*

$$0<\alpha<\alpha_{\text{crit}},$$

and unstable for

$$\alpha_{\text{crit}}<\alpha<1.$$

The sense in which stability is to be understood is this: As will be shown, the solution of equation (1) may be written in the form

$$\begin{aligned} x_n = (1-\alpha)&(\xi_n + b_{q+1}\xi_{n-1} + \cdots + b_{n+q-1}\xi_1) \\ &+ D_{q+1}b_{n-1} + D_q b_n + \cdots + D_1 b_{n+q-1}, \end{aligned} \qquad (3)$$

where $D_1, D_2, \cdots, D_{q+1}$ are constants depending upon the initial conditions, and $b_n=b_n(\alpha)$ is a certain sequence depending upon α. If the sequence b_n dampens exponentially to 0 as n tends to ∞, the sequence x_n is *stable*: otherwise, *unstable*. Observe that when $q=1$, $\alpha_{\text{crit}}=1$ by (2). Thus, in the case of linear prediction described above, the smoothing process (1) is stable for each allowable α. On the other hand, for $q=2$ (quadratic prediction) (2) yields $\alpha_{\text{crit}}=\frac{1}{2}$. When $q=3$, $\alpha_{\text{crit}}=\frac{1}{5}$. As $q\to\infty$, $\alpha_{\text{crit}}\to 0$.

Another matter considered in this paper is the variance σ_n^2 of the random variable[2] x_n for large n. Let $\xi_1, \xi_2, \xi_3, \cdots$ be independent and have a common variance σ^2. Let α be restricted to stable values. Put

$$\sigma_\infty^2 = \lim_{n\to\infty} \sigma_n^2.$$

(It is easy to see in this case that the limit exists.) It is desired to calculate the ratio σ_∞^2/σ^2 in order to compare the statistical behavior of x_n (for large n) with that of ξ_n. The calculation of this ratio is reduced to the determination of one of the unknowns of approximately $(q+2)/2$ linear equations, [$(q+2)/2$ if q is even, $(q+3)/2$ if q is odd] in as many unknowns as equations. The ratio σ_∞^2/σ^2 is a rational function of α; we shall explicitly exhibit this function for $q=1, 2, 3$.

A word should be added concerning the average $\bar{x}_n$ of x_n. It is undesirable that (1) should produce any systematic deviation of $\bar{x}_n$ from average value $\bar{\xi}_n$, which is presumably the true value of the datum. Since L_q is linear in its arguments it follows from (1) that

$$\bar{x}_n = \alpha L_q(\bar{x}_{n-1}, \bar{x}_{n-2}, \cdots, \bar{x}_{n-q-1}) + (1-\alpha)\bar{\xi}_n. \qquad (4)$$

Assume for the moment initial values $x_1=\xi_1$, $x_2=\xi_2$, $\cdots$, $x_{q+1}=\xi_{q+1}$ for (1). Thus $\bar{x}_1=\bar{\xi}_1$, $\bar{x}_2=\bar{\xi}_2$, $\cdots$, $\bar{x}_{q+1}=\bar{\xi}_{q+1}$. Now suppose that $\bar{\xi}_n$ is given as a polynomial in n of degree at most q. From the definition of L_q and the form of (4) it follows that $\bar{x}_n=\bar{\xi}_n$ for all n. That is, x_n and ξ_n have identical average values in case $\bar{\xi}_n$ is a polynomial of the type mentioned; and roughly, their averages will be close to the extent that such a polynomial approximation to $\bar{\xi}_n$ is accurate. If the initial values $x_1, x_2, \cdots, x_{q+1}$ are arbitrary, and α is in the range of stability the influence of initial values will ex-

[1] For a different method of sequential smoothing see N. Levinson, "The Wiener rms error criterion in filter design and prediction," *Jour. of Math. Phys.*, vol. 25, pp. 261–278; January, 1947. This paper also appears as Appendix B of the book by N. Wiener, "Extrapolation, Interpolation, and Smoothing of Stationary Time Series," John Wiley & Sons, Inc., New York, N. Y.; 1950.

[2] Here, of course, we think of $\xi_1, \xi_2, \xi_3, \cdots$ as random (i.e., statistical) variables (not sample values), and consequently the dependent quantity x_n is a random variable.

ponentially dampen out with increasing n, and the above comments concerning $\bar{x}_n$ remain valid, in effect, for sufficiently large n.

Quadratic Prediction

Instead of proceeding directly to the general case of q^{th} degree prediction it is proposed to treat the case $q=2$ first in order that the reader may have an opportunity to follow the solution to the problem in a context unencumbered by excessive notation. The general treatment in the next section will subsume the present case.

For quadratic prediction (1) becomes

$$x_n - \alpha L_2(x_{n-1}, x_{n-2}, x_{n-3}) = (1-\alpha)\xi_n$$

where L_2 is the value at n of the quadratic polynomial through the points $(n-3, x_{n-3})$, $(n-2, x_{n-2})$, $(n-1, x_{n-1})$. It is easy to see that

$$L_2(x_{n-1}, x_{n-2}, x_{n-3}) = 3x_{n-1} - 3x_{n-2} + x_{n-3}.$$

Thus the difference equation to be solved may be written

$$x_{n+3} - 3\alpha x_{n+2} + 3\alpha x_{n+1} - \alpha x_n = (1-\alpha)\xi_{n+3}, \quad (5)$$
$$n = 1, 2, 3, \cdots.$$

No particular initial values x_1, x_2, x_3 are to be specified.

Consider the associated homogeneous equation

$$v_{n+3} - 3\alpha v_{n+2} + 3\alpha v_{n+1} - \alpha v_n = 0. \quad (6)$$

Let b_n be the particular solution of (6) satisfying the initial conditions shown immediately below.

$$\begin{aligned} b_{n+3} - 3\alpha b_{n+2} + 3\alpha b_{n+1} - \alpha b_n &= 0 \\ b_0 = b_1 = 0, \qquad b_2 &= 1. \end{aligned} \quad (7)$$

Then the general solution of (5) is expressible in terms of b_n. First, by direct substitution it can be verified that

$$y_n = (1-\alpha)(\xi_n + b_3\xi_{n-1} + \cdots + b_{n+1}\xi_1)$$

is a particular solution of (5). Next, each of the sequences

$$\begin{aligned} v_n &= b_{n-1} \\ v_n &= b_n \\ v_n &= b_{n+1} \end{aligned}$$

is a solution of the homogeneous equation (6), with respective initial values

$$\begin{aligned} (v_1, v_2, v_3) &= (0, 0, 1) \\ (v_1, v_2, v_3) &= (0, 1, a) \\ (v_1, v_2, v_3) &= (1, b, c) \end{aligned}$$

for certain values a, b, c. Thus the general solution of (5) is

$$\begin{aligned} x_n = (1-\alpha)(\xi_n + b_3\xi_{n-1} + \cdots + b_{n+1}\xi_1) \\ + Db_{n-1} + Eb_n + Fb_{n+1} \end{aligned} \quad (8)$$

with D, E, F independent of n. The problem is now to determine b_n.

To solve (6) write

$$v_n = r^n$$

and determine r. Substitution in (6) yields the cubic

$$r^3 - 3\alpha r^2 + 3\alpha r - \alpha = 0,$$

which may be written

$$\left(\frac{r}{r-1}\right)^3 = -\frac{\alpha}{1-\alpha}.$$

Put

$$\beta = \frac{\alpha}{1-\alpha}, \qquad \gamma = \beta^{1/3}, \quad (9)$$

where γ is the positive cube root of β. Notice that β *is a strictly increasing function* for α in the range under consideration, $0<\alpha<1$.

The solutions of

$$z^3 = -\gamma^3$$

are

$$z_0 = -\gamma, \quad z_1 = \gamma e^{i\pi/3}, \quad z_2 = z_1^* = \gamma e^{-i\pi/3}$$

where z^* denotes the complex conjugate of z. The desired roots r are given by

$$\frac{r}{r-1} = z, \quad \text{i.e.,} \quad r = \frac{z}{z-1}.$$

Thus the roots are

$$\begin{aligned} r_0 &= \frac{\gamma}{1+\gamma} \\ r_1 &= \frac{\gamma(\gamma - 1/2 - i\sqrt{3/2})}{1-\gamma+\gamma^2}, \qquad r_2 = r_1^*. \end{aligned}$$

Putting

$$\rho_0 = \frac{\gamma}{1+\gamma}, \qquad \rho = \frac{\gamma}{(1-\gamma+\gamma^2)^{1/2}}, \quad (10a)$$

$$\cos\theta = \frac{\gamma - 1/2}{(1-\gamma+\gamma^2)^{1/2}}, \quad (10b)$$

we have

$$r_0 = \rho_0, \qquad r_1 = \rho e^{i\theta}, \qquad r_2 = \rho e^{-i\theta}.$$

The general solution of (6) is therefore

$$v_n = A\rho_0^n + B\rho^n \cos n\theta + C\rho^n \sin n\theta.$$

The particular solution b_n is obtained by specializing the coefficients A, B, C, but we shall not require the value of these coefficients to solve the problem of stability. In fact the condition for stability is

$$\rho_0 < 1 \quad \text{and} \quad \rho < 1.$$

The first condition is automatically satisfied from (10a) since $\gamma>0$. Writing the second condition as $\rho^2<1$ we obtain from (10a),

$$\gamma < 1, \quad \text{i.e.,} \quad \beta < 1;$$

but from (9) this is equivalent to

$$\alpha < 1/2,$$

that is to say,

$$\alpha_{\text{crit}} = 1/2,$$

as desired.

Let us turn attention now to the variance σ_n^2 of x_n. We suppose that the random variables $\xi_1, \xi_2, \xi_3, \cdots$ are independent and have common variance σ^2. We suppose further that α is in the range of stability. Then the last three terms of (8) are transients and we have

$$\frac{\sigma_\infty^2}{\sigma^2} = (1-\alpha)^2(1 + b_3^2 + b_4^2 + \cdots).$$

We introduce the notation

$$\begin{aligned} S_0 &= \sum_{j=0}^{\infty} b_j^2, & S_1 &= \sum_{j=0}^{\infty} b_j b_{j+1}, \\ S_2 &= \sum_{j=0}^{\infty} b_j b_{j+2}, & S_3 &= \sum_{j=0}^{\infty} b_j b_{j+3}. \end{aligned} \tag{11}$$

Then [using the second line of (7)],

$$\frac{\sigma_\infty^2}{\sigma} = (1-\alpha)^2 S_0.$$

To determine S_0 we may use (7). Multiply each side of the first line of (7) in turn by b_n, b_{n+1}, b_{n+2}, b_{n+3} and in each case sum from $n=0$ to $n=\infty$. Use of the initial conditions in the second line of (7) leads to

$$\begin{aligned} S_3 - 3\alpha S_2 + 3\alpha S_1 - \alpha S_0 &= 0 \\ S_2 - 3\alpha S_1 + 3\alpha S_0 - \alpha S_1 &= 0 \\ S_1 - 3\alpha S_0 + 3\alpha S_1 - \alpha S_2 &= 0 \\ S_0 - 3\alpha S_1 + 3\alpha S_2 - \alpha S_3 &= 1. \end{aligned}$$

Combining the first and fourth, and the second and third equations by addition we obtain

$$\begin{aligned} S_0 + S_3 &= \frac{1}{1-\alpha} \\ S_1 + S_2 &= 0. \end{aligned}$$

Eliminating S_3 and S_2 in the first two of the original equations leads to

$$\begin{aligned} (1+\alpha)S_0 - 6\alpha S_1 &= \frac{1}{1-\alpha} \\ 3\alpha S_0 - (1+4\alpha)S_1 &= 0. \end{aligned}$$

Thus,

$$S_0 = \frac{1+4\alpha}{(1-\alpha)(1-2\alpha)(1+7\alpha)},$$

and

$$\frac{\sigma_\infty^2}{\sigma^2} = \frac{(1-\alpha)(1+4\alpha)}{(1-2\alpha)(1+7\alpha)}.$$

Stability in the General Case

Let us first obtain an explicit expression for L_q of (1). Let $f(t)$ denote the polynomial of degree at most q for which

$$f(t) = x_t, \quad t = n-1, \quad n-2, \cdots, n-q-1.$$

By definition,

$$L_q(x_{n-1}, \cdots, x_{n-q-1}) = f(n).$$

We employ the operators Δ and E, where

$$\Delta f(t) = f(t+1) - f(t), \qquad Ef(t) = f(t+1).$$

Thus

$$\Delta = E - 1.$$

The polynomial $f(t)$ being of degree at most q, we have $\Delta^{q+1} f(t) = 0$ identically in t; i.e.,

$$(E-1)^{q+1} f(t) = 0.$$

Expanding the left side,

$$\left[E^{q+1} - \binom{q+1}{1} E^q + \cdots + (-1)^q \binom{q+1}{q} E + (-1)^{q+1}\right] f(t) = 0,$$

where

$$\binom{n}{k} = \frac{n!}{k!(n-k)!}.$$

Thus

$$f(t+q+1) - \binom{q+1}{1} f(t+q) + \cdots + (-1)^q \binom{q+1}{q} f(t+1) + (-1)^{q+1} f(t) = 0.$$

Put $t = n-q-1$. Then

$$L_q(x_{n-1}, \cdots, x_{n-q-1}) = -\left[-\binom{q+1}{1} x_{n-1} + \cdots + (-1)^q \binom{q+1}{q} x_{n-q} + (-1)^{q+1} x_{n-q-1}\right]. \tag{12}$$

We shall not use this result immediately.

Eq. (1) may be put in the form

$$x_{n+q+1} - \alpha L_q(x_{n+q}, \cdots, x_n) = (1-\alpha)\xi_{n+q+1}, \quad n = 1, 2, 3, \cdots. \tag{13}$$

As before, consider the homogeneous equation

$$v_{n+q+1} - \alpha L_q(v_{n+q}, \cdots, v_n) = 0 \tag{14}$$

and the particular solution

$$\begin{aligned} b_{n+q+1} - \alpha L_q(b_{n+q}, \cdots, b_n) &= 0 \\ b_0 = b_1 = \cdots = b_{q-1} &= 0, \quad b_q = 1. \end{aligned} \tag{15}$$

Let us verify that

$$y_n = (1 - \alpha)(\xi_n + b_{q+1}\xi_{n-1} + \cdots + b_{n+q-1}\xi_1)$$

is a particular solution of (13). Using the initial conditions of the b_n we may write

$$\begin{aligned} y_{n+q+1} &= (1 - \alpha)(\xi_{n+q+1} + b_{q+1}\xi_{n+q} + b_{q+2}\xi_{n+q-1} + \cdots) \\ y_{n+q} &= (1 - \alpha)(b_q\xi_{n+q} + b_{q+1}\xi_{n+q-1} + \cdots) \\ &\vdots \\ y_n &= (1 - \alpha)(b_0\xi_{n+q} + b_1\xi_{n+q-1} + \cdots). \end{aligned}$$

Forming the appropriate linear combination yields

$$\begin{aligned} y_{n+q+1} &- \alpha L_q(y_{n+q}, \cdots, y_n) \\ &= (1 - \alpha)[\xi_{n+q+1} - (b_{q+1} - \alpha L_q(b_q, \cdots, b_0))\xi_{n+q} \\ &\quad + (b_{q+2} - \alpha L_q(b_{q+1}, \cdots, b_1))\xi_{n+q-1} + \cdots] \\ &= (1 - \alpha)\xi_{n+q+1}, \end{aligned}$$

the second equation following from (15).

Each of the sequences

$$\begin{aligned} v_n &= b_{n-1} \\ v_n &= b_n \\ &\vdots \\ v_n &= b_{n+q-1} \end{aligned}$$

is a solution of (14) with respective initial values

$$\begin{aligned} (v_1, v_2, \cdots, v_{q+1}) &= (0, \cdots, 0, 0, 1) \\ (v_1, v_2, \cdots, v_{q+1}) &= (0, \cdots, 0, 1, -) \\ &\vdots \\ (v_1, v_2, \cdots, v_{q+1}) &= (1, -\cdots, -, -), \end{aligned}$$

where the blanks represent values of no particular concern. Thus, the general solution of (1) is

$$\begin{aligned} x_n = (1 - \alpha)(\xi_n + b_{q+1}\xi_{n-1} + \cdots + b_{n+q-1}\xi_1) \\ + D_{q+1}b_{n-1} + D_qb_n + \cdots + D_1b_{n+q-1}, \end{aligned}$$

as indicated earlier in (3).

To solve (14) put

$$v_n = r^n$$

and substitute into that equation. Using (12), we obtain

$$r^{n+q+1} + \alpha\left[-\binom{q+1}{1}r^{n+q} + \cdots + (-1)^{q+1}r^n\right] = 0,$$

i.e.,

$$(1 - \alpha)r^{q+1} + \alpha(r - 1)^{q+1} = 0.$$

Thus,

$$\left(\frac{r}{r-1}\right)^{q+1} = -\frac{\alpha}{1-\alpha}.$$

Put

$$\gamma = \left(\frac{\alpha}{1-\alpha}\right)^{1/(q+1)}, \qquad z = \frac{r}{r-1}.$$

Then the equation to be solved is

$$z^{q+1} = -\gamma^{q+1}. \tag{16}$$

Two cases may be distinguished: (1) q even, (2) q odd. In case (1), (16) has exactly one real root, namely, $-\gamma$; the remaining roots come in conjugate pairs. The corresponding values of r are

$$\rho_0 = \frac{\gamma}{1+\gamma}$$

and

$$\rho_k e^{\pm i\theta k}, \qquad k = 1, 2, \cdots, q/2.$$

Therefore b_n has the form

$$b_n = A\rho_0^n + \sum_{k=1}^{q/2} \rho_k^n(A_k \cos n\theta_k + B_k \sin n\theta_k).$$

In case (2), b_n has the form

$$b_n = \sum_{k=1}^{(q+1)/2} \rho_k^n(A_k \cos n\theta_k + B_k \sin n\theta_k).$$

Denote the roots of (16) by

$$z_1, z_2, \cdots, z_{q+1},$$

and the corresponding values of r by

$$r_1, r_2, \cdots, r_{q+1}$$

(q either odd or even). Then

$$z_j = w_j\gamma, \qquad j = 1, 2, \cdots, q+1,$$

where the w_j are the $q+1$ distinct roots of -1, i.e.,

$$w_j = e^{i\pi(2j-1/q+1)}, \quad j = 1, 2, \cdots, q+1.$$

Observe the transformation $z = r/(r-1)$ carries the interior of the unit circle in the complex r-plane into the half-plane to the left of the line $z = \frac{1}{2}$ in the complex z-plane. To see this write $z = x + iy$. Then

$$r = \frac{z}{z-1} = \frac{x+iy}{(x-1)+iy}$$

$$|r|^2 = \frac{x^2+y^2}{(x-1)^2+y^2}.$$

The inequality $|r| < 1$ is equivalent to $|r|^2 < 1$, which is the same as

$$\frac{x^2+y^2}{(x-1)^2+y^2} < 1, \quad \text{i.e.,} \quad x < \tfrac{1}{2},$$

as was to be shown.

Now the condition for stability is

$$\rho_j = |r_j| < 1, \quad j = 1, 2, \cdots, q+1.$$

In terms of the roots, z_j thus becomes

$$R(z_j) < \tfrac{1}{2},$$

where R denotes "real part." But this is equivalent to

$$\gamma < \frac{\frac{1}{2}}{\cos\frac{\pi}{q+1}};$$

that is to say,

$$\alpha < \frac{1}{\left(2\cos\frac{\pi}{q+1}\right)^{q+1}+1}.$$

The desired (2) is thereby established.

It is to be noted that this result on stability remains valid for a somewhat more general iteration procedure than that of (1). In fact consider a smoothing procedure

$$x_n = \alpha L_q(x_{n-1}, x_{n-2}, \cdots, x_{n-q-1}) + (1-\alpha)M_n(\xi_n, \xi_{n-1}, \cdots),$$

where M_n is any function of ξ_n and preceding data $\xi_{n-1}, \xi_{n-2}, \cdots$. This equation has the form

$$x_n = \alpha L_q(x_{n-1}, x_{n-2}, \cdots, x_{n-q-1}) + (1-\alpha)\eta_n,$$

with

$$\eta_n = M_n(\xi_n, \xi_{n-1}, \cdots).$$

Stability considerations for this equation are identical with those for (1).

Variance

Suppose that the random variables $\xi_1, \xi_2, \xi_3, \cdots$ are independent and have common variance σ^2. Let α be in the range of stability. Then, from (3)

$$\frac{\sigma_\infty^2}{\sigma^2} = (1-\alpha)^2\sum_{j=0}^{\infty} b_j^2 \equiv (1-\alpha)^2 S_0.$$

We shall employ (11) and the obvious extension of it to S_j, $j=0, 1, 2, \cdots$. Let us compute this ratio for the case of $q=3$ of cubic prediction. In this case, by (12),

$$L_3(x_{n+3}, x_{n+2}, x_{n+1}, x_n) = 4x_{n+3} - 6x_{n+2} + 4x_{n+1} - x_n,$$

so that, by (15),

$$b_{n+3} - 4\alpha b_{n+3} + 6\alpha b_{n+2} - 4\alpha b_{n+1} + \alpha b_n = 0 \qquad (17)$$

with initial conditions

$$b_0 = b_1 = b_2 = 0, \qquad b_3 = 1.$$

Multiply both sides of (17) in turn by b_n, b_{n+1}, b_{n+2}, b_{n+3}, b_{n+4}, and in each case sum from $n=0$ to $n=\infty$. We obtain

$$S_4 - 4\alpha S_3 + 6\alpha S_2 - 4\alpha S_1 + \alpha S_0 = 0$$
$$S_3 - 4\alpha S_2 + 6\alpha S_1 - 4\alpha S_0 + \alpha S_1 = 0$$
$$S_2 - 4\alpha S_1 + 6\alpha S_0 - 4\alpha S_1 + \alpha S_2 = 0$$
$$S_1 - 4\alpha S_0 + 6\alpha S_1 - 4\alpha S_2 + \alpha S_3 = 0$$
$$S_0 - 4\alpha S_1 + 6\alpha S_2 - 4\alpha S_3 + \alpha S_4 = 1.$$

Let us solve this system of equations for S_0 to illustrate the general technique of reducing the order of the system by approximately $\frac{1}{2}$. Combine the first and fifth and the second and fourth equations, by subtraction. Then

$$S_4 - S_0 = -\frac{1}{1-\alpha}$$
$$S_3 - S_1 = 0.$$

Eliminating S_4 and S_3 in the first three of the original equations yields

$$(1+\alpha)S_0 - 8\alpha S_1 + 6\alpha S_2 = \frac{1}{(1-\alpha)}$$
$$4\alpha S_0 - (1+7\alpha)S_1 + 4\alpha S_2 = 0$$
$$6\alpha S_0 - 8\alpha S_1 + (1+\alpha)S_2 = 0.$$

This third order system can be solved for S_0 and from this σ_∞^2/σ^2 obtained. The result is shown in the next paragraph.

The determination of S_0 for the cases $q=2$ and $q=3$ illustrates the general method that can be used for the solution of S_0. One obtains a system of $q+2$ equations in $S_0, S_1, \cdots, S_{q+1}$ by using (15). Combining the first and $(q+2)^{th}$ equation, the second and $(q+1)^{th}$ equation, etc., by either subtraction (q odd) or addition (q even), enables us to write

$$S_{q+1} = \pm\left(S_0 - \frac{1}{1-\alpha}\right), \qquad S_q = \pm S_1,$$
$$S_{q-1} = \pm S_2, \cdots$$

(upper sign for q odd and lower sign for q even). The variables $S_{q+1}, S_q, \cdots$ can then be eliminated and the system of equations reduced by approximately one-half. In summary we tabulate the results for $q=1, 2, 3$.

$$\frac{\sigma_\infty^2}{\sigma^2} = \frac{1+\alpha}{1+3\alpha} \qquad (q=1),$$
$$\frac{\sigma_\infty^2}{\sigma^2} = \frac{(1-\alpha)(1+4\alpha)}{(1-2\alpha)(1+7\alpha)} \qquad (q=2),$$
$$\frac{\sigma_\infty^2}{\sigma^2} = \frac{1+8\alpha-25\alpha^2}{(1-5\alpha)(1+15\alpha)} \qquad (q=3).$$

Notice that for $q=2$ and $q=3$ the ratio approaches $+\infty$ at the respective critical values $\frac{1}{2}$ and $\frac{1}{5}$ [see (2)].

Contributors

J. C. Alrich (A'50–M'55) was born in Los Angeles, Calif., on June 16, 1923. He attended the University of California at Los Angeles and the University of California at Berkeley, from which he was graduated in 1948 with the B.S. degree in electrical engineering. For a year and a half he was associated with Bendix Aviation Corp. as an engineer in telemetering, and for the following year and a half with Fairchild Camera and Instrument Corp. as an engineer in the development of film potentiometers.

In 1951 he joined the newly-formed Computer Division of Consolidated Engineering Corp. He is at present an engineer with ElectroData Corp., an affiliate of Consolidated Engineering formed in 1954.

Mr. Alrich is a member of Tau Beta Pi and Eta Kappa Nu.

W. Karush was born in Chicago, Ill., on March 1, 1917. He received his Ph.D. in mathematics from the University of Chicago in June, 1942.

From 1942 to 1943 he worked in Washington, D. C. on problems of exterior ballistics; the following two years, 1943–1945, he spent as an applied mathematician with the Metallurgical Laboratory at the University of Chicago. In 1945 he joined the faculty of the University of Chicago, where he is now an associate professor of mathematics.

Mr. Karush was a member of the Institute for Numerical Analysis of the University of California at Los Angeles in 1949–1950. He spent six months in 1953 with the Computer Systems Department of Hughes Aircraft Company. Most recently he has been a mathematical consultant for the Computing Systems Division of the Ramo-Wooldridge Corp.

Dr. Karush is a member of the American Mathematical Society and the Institute of Management Sciences.

W. A. Malthaner (SM'51) was born in Columbus, Ohio, on July 3, 1915. He received the B.E.E. degree from Rensselaer Polytechnic Institute in 1937. Immediately thereafter he joined Bell Telephone Laboratories, where for several years he was concerned with circuit testing and development. He also devoted time to research on subscriber signaling arrangements and the associated central office switching systems.

During World War II, Mr. Malthaner did government contract work on automatic fire control systems and fire control radar. Since 1945 he has been interested in new automatic telephone central office systems, subscriber dialing and interoffice signaling systems.

Mr. Malthaner is a member of Sigma Xi, Tau Beta Pi and an associate of the A.I.E.E.

H. E. Vaughan (SM'52) was born in Yonkers, N. Y., on February 3, 1912. He received the B.S. degree in civil engineering from Cooper Union in 1933, five years after joining Bell Telephone Laboratories' Transmission Research Department. He devoted several years to studies of voice-operated devices and the effect of speech and noise on voice frequency signaling systems.

In 1941 he worked on special Army and Navy projects, including anti-aircraft computers and fire control radar. Transferring to switching research in 1945, he has since been engaged in work on high-speed signaling devices, and is currently concerned with development of future switching systems.

C. L. Wanlass (S'49–A'51) received the B.S. degree in electrical engineering in 1950 and the M.S. degree in 1951, from the University of California at Berkeley, Calif. In 1951 he joined the research and development facilities of the North American Aviation Co., where he was in charge of research work on digital computer circuitry for two vacuum tube computers and on all transistor digital computers.

Recently he joined the technical staff of the Ramo-Wooldridge Corp. in Los Angeles, Calif.

Mr. Wanlass is a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Xi.

J. M. Wier (A'50) was born in Amsterdam, Mo., on March 2, 1924. After spending three years in the U. S. Army, he attended Iowa State College, receiving the B.S. degree in 1949 and the M.S. degree in 1950, both in electrical engineering.

Since 1950 he has been associated with the Digital Computer Laboratory of the University of Illinois, first as a research assistant and later as a research associate. He has worked on the Williams memories for the Ordvac and the Illiac, and has carried out experimental work on various other types of memories and computer components.

He is a member of Tau Beta Pi, Eta Kappa Nu, Pi Mu Epsilon, and Phi Kappa Phi.

PGEC News

Message from the Chairman

The purpose of this message is to describe briefly several of the current activities of the PGEC. It is hoped that this will convey some idea of the work performed by the mechanisms of this organization. The communication of this information to you is coupled with an invitation to participate actively wherever you note something of interest to you.

Sectional Activities—The Sectional Activities Committee has several functions, all of which have to do with the PGEC chapters. These functions include (a) the establishment of new chapters in areas where computer activity warrants the existence of a chapter, (b) liaison between the national PGEC organization and the chapters, (c) preparation of the news column in the Transactions, and (d) special projects that aid the chapters.

The chairmen of the eleven PGEC chapters form the body of the Sectional Activities Committee, serving as natural communication links between the national and local PGEC organizations. It appears, at this writing, that a new chapter may be forming soon in Baltimore. This committee has recently compiled the results of a questionnaire surveying the chapters. In addition to organizational and financial matters, this survey indicates (a) a moderate amount of joint activity with ACM, AIEE-CDG, and SIAM, and (b) several chapters are sponsoring or co-sponsoring special lecture series, sessions at conventions, panel discussions, and experimental meetings. The results of this survey may be obtained by contacting the Chairman of the Sectional Activities Committee.

A fund of $1,000 was set aside last year by the National Administration Committee for the use of the chapters in conducting experimental meetings or other activities aimed at furthering the well-being of computer people in their areas. A goodly portion of this fund remains unused at this writing.

Standards—The rapid growth of the electronics industry into new areas has made it necessary for the IRE technical committees to reexamine their standards activities. Some areas are receiving little or no standards attention, while others are overlapped by two or more technical committees formerly covering distinct fields. A special committee has been formed to examine this situation, and this committee has asked the aid of the professional groups in determining the unattended and overlapped activities. The PGEC responded by using its liaison system to communicate with businesses and universities known to be active in computer work. The response was light. The information and recommendations obtained have been communicated to the appropriate IRE committees.

Student Relations Activity—The December issue of the IRE Student Quarterly in-

cluded two articles supplied by the PGEC, one on the PGEC itself and the other on a new photographic storage device. It is hoped that you will see fit to supply our Publications Committee with other such short news articles for inclusion in the Student Quarterly.

The Student Relations Committee has established two new PGEC activities designed to stimulate student interest in the computer field. The first is the establishment of an annual monetary prize for the best Student Quarterly article on computers written by a student. In addition, computer problems will be presented in the Student Quarterly, and a prize awarded for the best solution submitted by a student.

The Student Relations Committee is currently studying the possibility of establishing a computer scholarship sponsored by the PGEC.

Publications—The PGEC is attempting to establish a special annual subscription rate for the PGEC TRANSACTIONS for bona fide members of certain professional societies with which it is hoped to make reciprocal arrangements. This plan is now being worked out under the supervision of the Publications Committee for presentation to the IRE.

It is planned to discontinue the institutional listings in the PGEC TRANSACTIONS.

The Administrative Committee has approved the establishment of awards of $50.00 each for the best three papers appearing in the TRANSACTIONS each year.

Harry T. Larson
Chairman
IRE Professional Group on
Electronic Computers

CHAPTER ACTIVITIES

New York—The October meeting of this chapter was held at the analog-digital computer installation of the Reeves Instrument Company. The Elecom Computers were described at the November meeting, and the "Feasibility of an All-Magnetic Digital Computer" was discussed by Isaac L. Auerbach, Burroughs, in December. A lecture series entitled "Digital Computers in Control Systems" was jointly sponsored by the AIEE during February and March.

Dallas-Fort Worth—Extremely active in the analog computer field, this chapter is compiling a directory of electronic differential analyzer installations and is also proposing a National Simulation Conference in January, 1956, at Dallas. For information on either topic, get in touch with the Chapter Chairman, Louis B. Wadel, 3905 Centenary Drive, Dallas 25, Texas.

Baltimore—Those interested in the formation of the Baltimore Chapter of the PGEC are urged to get in touch with Mr. George W. Oberle, Glenn L. Martin Co., Baltimore 3, Md.

MEETING NOTICES

Mar. 1– 3—Western Joint Computer Conference, Hotel Statler, Los Angeles, Calif.
Mar. 21–24—IRE National Convention, Waldorf-Astoria and Kingsbridge Armory, New York, N. Y.
Apr. 13–15—AIEE Southern District Meeting, St. Petersburg, Fla.
May 4– 6—AIEE Middle Eastern District Meeting, Columbus, Ohio.
May 18–20—IRE-AIEE-IAS-ISA National Telemetering Conference, Hotel Morrison, Chicago, Ill.
May 26–27—IRE-AIEE-RETMA-WCEMA Electronics Components Conference, Los Angeles, Calif.
Sept. 14–16—Annual National Convention, ACM, University of Pennsylvania, Philadelphia, Pa.

COMPUTER PAPERS FOR 1955 WESCON

The annual Western Electronics Show and Convention (WESCON) will be held in San Francisco, from August 24–26, 1955. It is sponsored jointly by the West Coast Electronic Manufacturers' Association and the San Francisco and Los Angeles Sections representing the Seventh Region of the I.R.E.

Papers for this convention should be mailed to Dr. W. A. Edson at the Applied Electronics Laboratory, Stanford, Calif. In addition to the title, authors are asked to submit an abstract of approximately 200 words, suitable for reproduction in the program, and either the complete manuscript or sufficient additional information to permit evaluation by the Technical Program Committee. Early submission of papers is desired, the final deadline being May 1. This is the latest date which is operationally feasible, and papers received thereafter cannot be considered.

Authors should say if demonstrations are planned and should indicate what facilities, such as slide or movie projectors, power sources, etc., are required.

Review of Electronic Computer Progress During 1954

DAVID R. BROWN†, EDITOR

THE ELECTRONIC computer field continues to expand at a rapid rate. New developments, applications, and publications are too numerous for one person to keep informed of all aspects. In this review a complete report will not be attempted, but some highlights and selected references will be reported.

(1) B. V. Bowden, Ed., "Faster Than Thought, A Symposium on Digital Computing Machines," Sir Isaac Pitman and Sons, London; 1953.

SYSTEMS

Business Applications

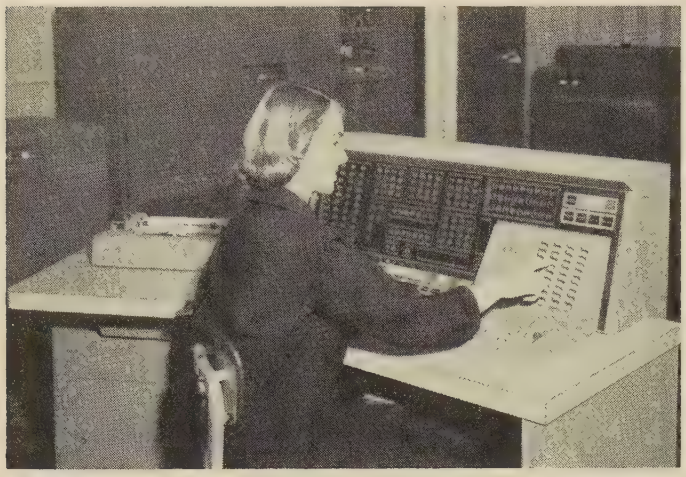
Business applications of electronic digital computers have sharply increased, attracting much attention.

† Lincoln Laboratory, Mass. Inst. Tech., Lexington, Mass.

(2) M. E. Davis, "Use of electronic data-processing systems in the life insurance business," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 11–17; December 8–10, 1953.
(3) O. Whitby, "The automatic handling of business data," *Proc. of the Western Computer Conference*, Los Angeles, California, pp. 75–79; February 11–12, 1954.
(4) A. St. Johnston and S. L. H. Clarke, "Applications of high-speed electronic computers to business-accounting problems," *Jour. Brit. I.R.E.*, vol. 14, pp. 293–302; July, 1954.

The different electronic systems used for these applications have a wide range of size, complexity, and cost.

A model of the IBM Type 702, a large-scale electronic data-processing machine for business use, has been in use in the laboratory for the greater part of the year. It is a serial, stored-program, decimal machine. Several unusual logical features, including variable word lengths and variable record lengths, are provided to aid in programming accounting problems. The 702



Operator's console of the IBM Type 702 data-processing machine.

incorporates magnetic tape, electrostatic memory supplemented by magnetic drums, punched-card document input and output, and a page printer. Later in the year the Type 705 was announced as a successor to the Type 702. It has about twice the over-all speed, a magnetic-core memory of twice the size, and several new instruction features.

(5) C. J. Bashe, W. Buchholz, and N. Rochester, "The IBM type 702, an electronic data processing machine for business," presented at the ACM Meeting, Ann Arbor, Michigan, June 23, 1954; to be published in the *Jour. Ass. Computing Machinery.*

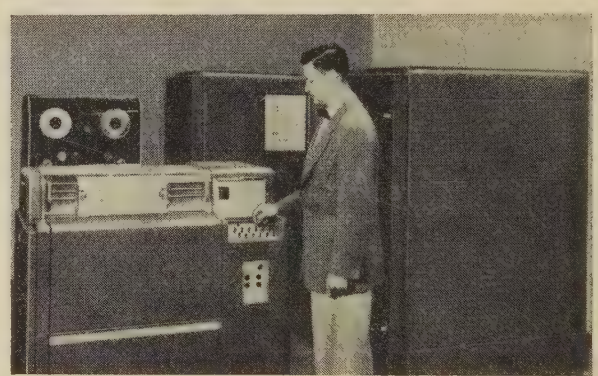
Business installations of the Remington Rand UNIVAC electronic data-processing system include the General Electric Company in Louisville, Kentucky, Metropolitan Life Insurance Company in New York, and the National Tube Division of US Steel in Pittsburgh. The first installation, at Appliance Park, newly constructed home of General Electric's major appliance division, is to process payroll, labor distribution, material scheduling, and inventory control. Plans call for the additional processing of commercial service, billing, and general and cost accounting by the end of 1954. Compared with conventional methods in the same administrative areas, annual savings of $500,000 are estimated in performing these initial functions alone. UNIVAC's potential, however, permits planning to enlarge its scope considerably. One of the computer's most important eventual uses at Appliance Park is expected to be in the compilation of sales statistics and the preparation of market forecasts for division and product department management.

In May of 1954, Remington Rand's ERA Division installed an ore-car data-processing system for the Great Northern Railroad in northern Minnesota. This system contains electromechanical data-gathering, storing, and computing equipment for assembling, processing, transmitting, and recording data relative to the automatic weighing of ore cars which are in motion.

The Burroughs Corporation has announced the E101 desk-size electronic digital computer. This is a general-purpose computer with a magnetic-drum memory having a 100-word capacity. Data are introduced into the E101 through a keyboard and printed from the machine at speeds up to 24 characters per second. The machine automatically selects the proper columns to print answers. It is flexible with respect to the size and shape of the document used and will handle up to six carbon copies. Results are immediately available in usable form.

Telecomputing Corporation has announced a large-capacity, random-access, magnetic memory designed for industrial and business data-processing problems. Christened "MASS" (for multiple-access storage system), the unit has a capacity of 120 million bits and an access time of less than one second. Facilities for read-in, read-out, and updating are provided. The first MASS will be delivered to Wright Air Development Center and will be used in a study of Air Force inventory control problems.

(6) A. A. Cohen, "The role of general purpose digital computers in automatic control and information systems," 1954 IRE Convention Record, Part 4, Electronic Computers and Information Theory, pp. 82–86.
(7) J. M. M. Pinkerton, E. J. Kaye, E. H. Lenaerts, and G. R. Gibbs, "Leo (Lyons Electronic Office)," *Electronic Eng.* (London), vol. 26, pp. 284–291, 335–341, 386–392; July, August, September, 1954.



High-speed printer of the UNIVAC system for handling large volume output. It is capable of printing 600 lines per minute.

Control Applications

The application of computers to both open- and closed-loop control systems offers a field of tremendous potentiality. The DIGITAC, the first airborne control system employing a general-purpose digital computer, was announced early during the year. This system is an automatic navigation and weapons control system that has been developed and successfully flight tested. The digital computer employed in the system is a general-purpose relative-address machine with a serial magnetic-drum memory. The clock frequency is 100 kilocycles per second and the memory capacity is approximately 1,200 words of 16 bits plus sign. The computer includes 260 electron tubes, 1,300 germanium diodes, and occupies a volume of about 5 cubic feet.

(8) R. B. Conn, "Digital computers for linear real-time control systems," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 33–37; December 8–10, 1953.
(9) V. I. Weihe, "Computer applications in air traffic control," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 18–21; December 8–10, 1953.
(10) D. W. Burbeck, E. E. Bolles, W. E. Frady, and E. M. Grabbe,

"The DIGITAC airborne control system," *Proc. of the Western Computer Conference*, pp. 38–44; Los Angeles, California, February 11 and 12, 1954.

Scientific Applications

The development of bigger and better large-scale general-purpose computers intended primarily for scientific applications continues at a rate which demonstrates that the number of organizations which need such a computer has been underestimated.

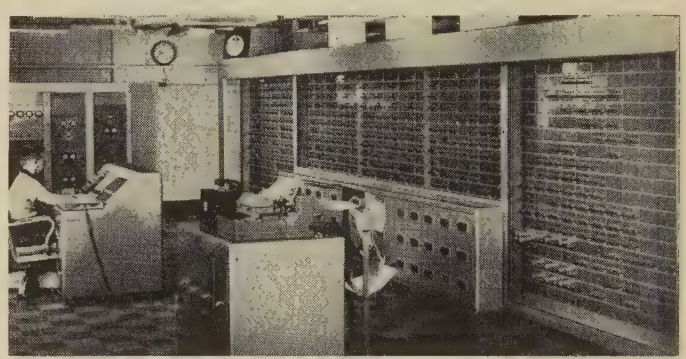
During 1954, IBM announced several additions to its line of electronic data-processing machines following their release in 1953 of the Type 701, a high-speed, parallel, binary machine for scientific computation. At the end of 1954, there were eighteen of the Type 701 machines installed and in full operation. A model of a new machine, Type 704, which is intended for the same general applications, has meanwhile been placed in operation in the laboratory and is scheduled for early production. The Type 704 contains many new features including index registers, logical addition and multiplication, and built-in floating-point arithmetic. It uses a magnetic-core memory of 4,096 words, faster magnetic drums, and faster magnetic-tape. The 704 is at least twice as fast as the 701. In many applications the new features combine to give an even higher over-all speed. Floating-point addition, for instance, is twenty times as fast on the 704 as on the 701, where programmed floating-point addition must be used.

Another IBM computer for scientific problems was announced and demonstrated on December 2, 1954. This is the Naval Ordnance Research Calculator (NORC) built by IBM expressly for the Navy Bureau of Ordnance. According to its designers, it is the fastest existing large-scale computer. It executes about 15,000 three-address stored-program instructions per second including automatic address modification and floating point, operating directly in the decimal system and employing some unusual checking features. Two words of 13 decimal digits (plus a 2-digit exponent and sign) are multiplied in 31 microseconds exclusive of access to the electrostatic memory. The programmer has the option of using floating-point operation or specifying the decimal-point position. The NORC has magnetic-tape input and output of unusually high density and speed attaining a rate of 70,000 decimal digits per second.

Three ERA 1102 digital computer systems were built for the USAF Arnold Engineering Development Center. Each system is operated on line to reduce experimental data to tabular and plotted form. As many as 250 sensing transducers are scanned under computer-programmed control during each data-reduction cycle. The first two of these were delivered in 1954.

During 1954, ERA 1103 computer systems were installed and put into operation on several new types of work, including engineering design computations and data reduction. A comprehensive computer-programmed maintenance technique applicable to the ERA 1103 computer system was developed. During the first six months of 1954 this technique increased the average hours of production time between unscheduled interruptions from 18 to 41 hours.

(11) S. R. Cray, "Computer-Programmed Preventive Maintenance for Internal Memory Sections of the ERA 1103 Computer System," presented at the Western Electronic Show and Convention, August 25–27, 1954, Los Angeles, California.



NAREC installation at the Naval Research Laboratory, Washington, D. C.

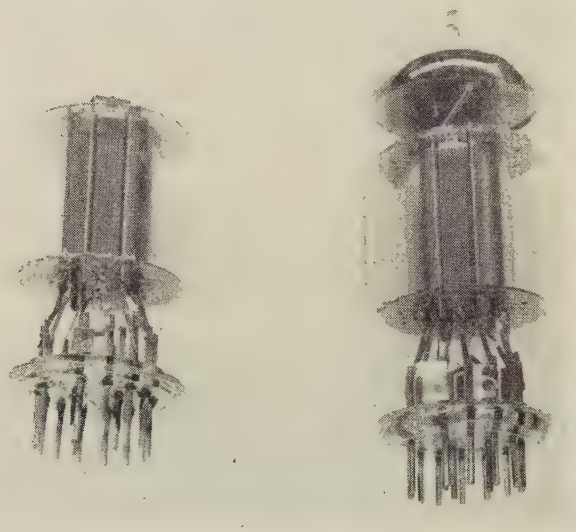
Burroughs E101 desk-size computer.

The NAREC has been placed in operation with its electrostatic-storage system during the past year. This computer, located at the Naval Research Laboratory, Washington, D. C., is a high-speed, asynchronus, 45-bit parallel machine used for mathematical calculations and data reduction associated with many scientific problems of the laboratory. It is equipped with 1,024 words of electrostatic storage and at present 1,536 words of magnetic-drum storage. Early in 1955, the drum capacity will be increased to 8,192 words of storage. Punched paper and magnetic tape are used for input and output with an auxiliary photoelectric punched paper-tape reader, the Flexowriters operating either directly from the computer output or on a delayed basis as read from slowly-moving magnetic-tape playback. The NAREC is built completely on a plug-in chassis system and is provided with automatic checking within the arithmetic section, both of which aid in the main-

tenance problems and location of faults. The electrostatic storage utilizes three standard three-inch cathode ray tubes for each forty-five digits, a system that has proven valuable in avoiding moderate storage-surface blemishes and has increased the usable read-around ratio by an appreciable amount.

At the Ballistic Research Laboratories, Aberdeen Proving Ground, the ENIAC completed its eighth year as an operating machine in February, 1954. A number of basic improvements during this period has enabled the ENIAC to remain efficient of operation.

(12) A. L. Leiner and S. N. Alexander, "System organization of the DYSEAC," *Trans. I.R.E.*, vol. EC-3, pp. 1–10; March, 1954.
(13) D. B. G. Edwards, "The Manchester University high-speed digital computer," *Jour. Brit. I.R.E.*, vol. 14, pp. 269–278; June, 1954.



Burroughs beam-switching tube, a high-vacuum device with ten discrete outputs capable of operating at frequencies greater than 1 megacycle per second.

Operating Experience

Operating experience has been reported for a number of large-scale systems.

(14) P. D. Shupe and R. A. Kirsch, "SEAC—review of three years of operation," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 83–90; December 8–10, 1953.
(15) B. Loveman, "Reliability of a large REAC installation," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 53–57; December 8–10, 1953.
(16) R. Kopp, "Experience on the Air Force UNIVAC," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 62–66; December 8–10, 1953.
(17) R. B. House, "Reliability experience on the OARAC," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 43–44; December 8–10, 1953.
(18) C. R. Williams, "A review of the ORDVAC operating experience," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 91–95; December 8–10, 1953.
(19) W. G. Bouricius, "Operating experience with the Los Alamos 701," *Proc. of the Eastern Joint Computer Conference*, Washington D. C., pp. 45–47; December 8–10, 1953.
(20) F. J. Murray, "Acceptance test for Raytheon Hurricane computer," *Proc. of the Eastern Joint Computer Conference*, Washington D. C., pp. 48–52; December 8–10, 1953.

General

Selected references dealing with computer systems are listed.

(21) J. Smagorinsky, "Data processing requirements for numerical weather prediction," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 22–30; December 8–10, 1953.
(22) J. M. Salzer, "Frequency analysis of digital computers operating in real time," PROC. I.R.E., vol. 42, pp. 457–466; February, 1954.
(23) A. L. Freedman, "Elimination of waiting time in automatic computers with delay-type stores," *Proc. Cambridge Phil. Soc.*, vol. 50, part 3, pp. 426–438; July, 1954.
(24) H. H. Goldstine, "Some remarks on logical design and programming checks," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 96–98; December 8–10, 1953.
(25) J. W. Mauchly, "The advantages of built-in checking," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 99–101; December 8–10, 1953.
(26) S. N. Alexander and R. D. Elbourn, "National Bureau of Standards performance tests," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 58–61; December 8–10, 1953.
(27) E. L. Braun, "Design features of current digital differential analyzers," 1954 IRE CONVENTION RECORD Part 4, "Electronic Computers and Information Theory," pp. 87–97.
(28) W. E. Scott and A. D. C. Haley, "Some comparisons between analogue and digital computers," *Jour. Brit. I.R.E.*, vol. 14, pp. 476–486; October, 1954.

COMPONENTS AND TECHNIQUES

New Components and Circuits

New components, such as the transistor and the magnetic core, are being used to replace electron tubes and make more reliable and compact systems possible. Techniques to use these new components are being investigated intensively in the laboratory but no operational systems employing these techniques have reached the users of computing systems.

An experimental all-transistor calculator, which has the functions of the familiar IBM Type 604 electron-tube calculator, including input and output, was demonstrated publicly on October 7, 1954. This was probably the first showing of an entirely transistorized calculator in operation, complete with input and output. The transistors are of the junction type and mounted on pluggable units with printed wiring. No electron tubes are used in this experimental machine, which is about half the size and requires only 5 per cent of the power production-line electron-tube counterpart.

The Minnesota Electronics Corporation reports operation of an engineering model of an all-magnetic-core data-processing system.

Both transistor circuits and magnetic-core circuits appear promising and large systems employing these techniques can be expected during the next few years.

(29) R. H. Baker, I. L. Lebow and R. E. McMahon, "Transistor shift registers," PROC. I.R.E., vol. 42, pp. 1152–1159; July, 1954.
(30) C. Huang, E. Slobodzinski and B. White, "Transistor shift registers," 1954 IRE CONVENTION RECORD, Part 4, "Electronic Computers and Information Theory," pp. 140–144.
(31) E. U. Cohler, "Transistor flip-flops for high-speed digital computers," presented at the Western Electronic Show and Convention, August 25–27, 1954, Los Angeles, California.
(32) V. L. Newhouse, "Review of magnetic and ferroelectric computing components," *Electronic Eng.* (London), vol. 26, pp. 192–199; May, 1954.
(33) S. Guterman, R. D. Kodis, and S. Ruhman, "Circuits to perform logical and control functions with magnetic cores," 1954 IRE CONVENTION RECORD, Part 4, "Electronic Computers and Information Theory," pp. 124–132.
(34) R. C. Minnick, "Magnetic switching circuits," *Jour. Appl. Phys.*, vol. 25, pp. 479–485; April, 1954.
(35) B. Moffat, "Saturable transformers as gates," *Electronics*, vol. 27, pp. 174–176, 178; September, 1954.
(36) D. A. Buck and W. I. Frank, "Nondestructive sensing of magnetic cores," *Trans. AIEE, Part I*, "Communication and Electronics," vol. 72, pp. 822–830; January, 1954.
(37) A. Papoulis, "Nondestructive read-out of magnetic cores," PROC. I.R.E., vol. 42, pp. 1283–1288; August, 1954.
(38) R. W. Rutishauser, "Ferroresonant flip-flop design," *Electronics*, vol. 27, pp. 152–153; May, 1954.

(39) S. Guterman and R. D. Kodis, "Magnetic core selection systems," 1954 IRE Convention Record, Part 4, "Electronic Computers and Information Theory," pp. 116–123.

An interesting high-speed computer circuit was developed at the Bureau of Standards using neither magnetic cores nor transistors, but using the hole storage in a diode as the basis for operation.

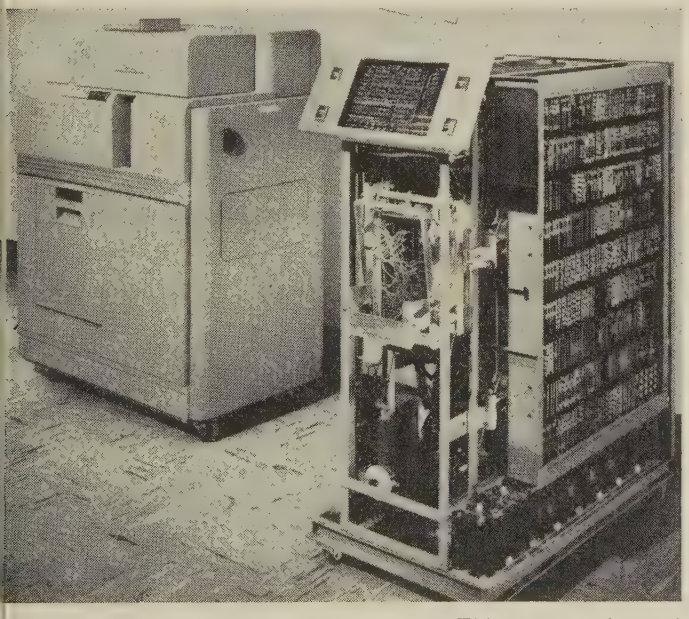
(40) A. W. Holt, "Diode amplifier," *Tech. Bull. Nat. Bur. Stand.*, vol. 38, pp. 145–148; October, 1954.

Some references to other techniques are listed.

(41) D. A. Huffman, "Synthesis of sequential switching circuits," *Jour. Frank. Inst.*, vol. 257, pp. 161–190, 275–303; March, April, 1954.
(42) A. D. Booth and A. D. Holt, "Selenium rectifier in digital computer circuits," *Electronic Eng.* (London), vol. 26, pp. 348–355; August, 1954.
(43) J. J. Bruzac, "New flip-flop chain circuits used in computers for counting to base 10 and base 12," *Onde Elec.*, vol. 34, pp. 59–62; January, 1954.
(44) J. R. Stock, "An arithmetic unit for automatic digital computers," *Z. Angew. Phys.*, vol. 5, pp. 168–172; March 15, 1954.
(45) N. Zimbel, "Packaged logical circuitry for a 4 MC computer," 1954 IRE Convention Record, Part 4, "Electronic Computers and Information Theory," pp. 133–139.
(46) G. Piel, "Electronic-circuit technique for a high-speed computer," *Onde Elec.*, vol. 34, pp. 38–46; January, 1954.

Memory Techniques

The magnetic-core memory appears to provide a very successful high-speed memory technique. A 4,096-word magnetic-core memory in MIT's Memory Test Computer is now operated on a routine basis with a read-rewrite cycle of 6 microseconds. A number of magnetic-core memories are being constructed to replace electrostatic storage in existing general-purpose computers. A 4,097-word memory is to be installed in Rand Corporation's JOHNNIAC at the end of 1954. The first ERA 1103 computer system with coincident-current magnetic-core memory was delivered to a government user and placed in operation in November 1954.

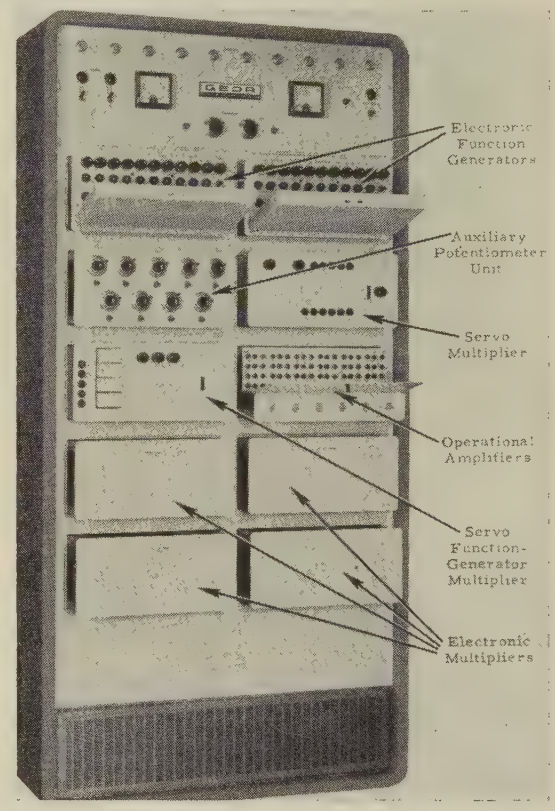


IBM's experimental all-transistor calculator. This new experimental computer is composed of a high-speed punching unit (left) and the transistorized calculating unit at right. The calculating unit is uncovered to show the bank of printed wiring panels on which the transistors are mounted. This "all-transistor" unit is approximately one-half the size of a vacuum-tube unit of comparable capacity and requires only 5 per cent as much power.

(47) W. N. Papian, "The MIT magnetic-core memory," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 37–42; December 8–10, 1953.
(48) J. R. Freeman, "Pulse Response of Ferrite Memory Cores," presented at the Western Electronic Show and Convention, August 25–27, 1954, Los Angeles, California.

For descriptions of other memory techniques see:

(49) G. L. Hollander, "Fundamentals of Photographic Data Storage," presented at the Western Electronic Show and Convention, August 25–27, 1954, Los Angeles, California.
(50) J. M. Wier, "Reliability and characteristics of the Illiac electrostatic memory," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 72–76; December 8–10, 1953.
(51) R. J. Klein, "Automatic beam current stabilization for Williams tube memories," *Trans. I.R.E.*, vol. EC-2, pp. 8–10; December, 1953.
(52) R. D. Ryan, "A mercury delay-line memory unit," Proc. I.R.E. (Australia), vol. 15, pp. 89–95; April, 1954.
(53) D. R. Quested and A. D. Booth, "Phonic wheel generator for position indication in digital computer magnetic drum storage," *Jour. Sci. Instr.*, vol. 31, pp. 357–360; October, 1954.

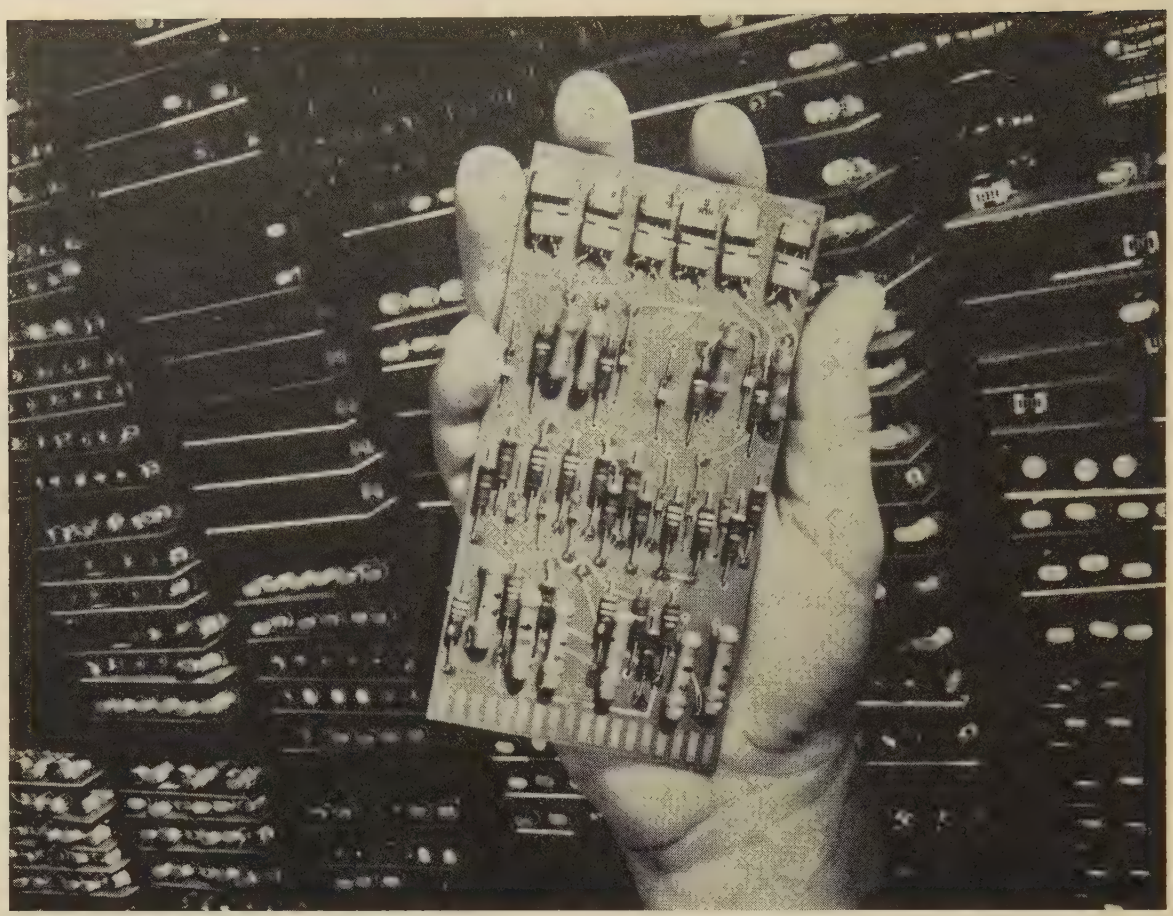


Goodyear Aircraft Corporation's N3GEDA analog computer.

Component Reliability

Component reliability is of primary importance in the design and operation of large electronic computers. Information on reliability is difficult to obtain and difficult to present. More effort is being directed toward understanding and improving reliability.

On May 1, 1954, TRADIC (Transistor Digital Computer) was put on life test at BTL and since then has been running 24 hours a day, 7 days a week. The TRADIC computer was designed for military applications and has a restricted memory capacity. It is, however, a general purpose computer and runs at a megacycle rate. It uses 700 transistors and 11,000 diodes. During its 5,500 hours of operation, a transistor replacement rate of 0.10 per cent per thousand hours and a diode re-



Printed wiring panels used in IBM's all-transistor calculator. These printed wiring panels simplify production and maintenance and also effect a great reduction in space requirements. Devices mounted on the panel include transistors (extreme left), diodes, and resistors. The model contains 595 such panels.

placement rate of 0.01 per cent per thousand hours have been established.

(54) J. A. Goetz and H. J. Geisler, "Electron tube and crystal diode experience in computing equipment," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 67–72; December 8–10, 1953,
(55) D. W. Sharp, "Electron tube performance in some typical military environments," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 77–83; December 8–10, 1953.
(56) L. D. Whitelock, "Methods used to improve reliability in military electronics equipment," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 31–33; December 8–10, 1953.
(57) L. Knight, "Valve reliability in digital calculating machines," *Electronic Eng.* (London), vol. 26, pp. 9–13; January, 1954.
(58) E. B. Ferrell, "Reliability and its relation to suitability and predictability," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 113–116; December 8–10, 1953.
(59) J. C. Chapman and W. W. Wetzel, "Recent progress in the production of error-free magnetic computer tape," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 102–104; December 8–10, 1953,
(60) M. VanBuskirk, "Reliability of electrolytic capacitors in computers," *Proc. of the Eastern Joint Computer Conference*, Washington, D. C., pp. 105–108; December 8–10, 1953.
(61) J. Marsten, "Resistor reliability—whose responsibility?" *Proc. of the Eastern Joint Computer Conference*, pp. 109–112; December 8–10, 1953.

Input and Output Techniques

As the field of application of electronic computers increases, the many different input-output requirements result in a variety of techniques.

(62) F. Raasch, "A progressive code digital quantizer," *Trans. AIEE*, Part I, "Communication and Electronics," vol. 72, pp. 567–571; November, 1953.
(63) S. Lubkin, "Electrostatic reading of perforated media," 1954 IRE Convention Record, Part 4, "Electronic Computers and Information Theory," pp. 106–108.
(64) R. A. Langevin, "A germanium tape reader," 1954 IRE Convention Record, Part 4, "Electronic Computers and Information Theory," p. 105.
(65) L. P. Retzinger, "An Input-Output System for a Digital Control Computer," presented at the Western Electronic Show and Convention, August 25–27, 1954, Los Angeles, California.
(66) C. W. Fritze, "Tape recorder stores computer output," *Electronics*, vol. 27, pp. 166–169; July, 1954.
(67) T. Kilburn and E. R. Laithwaite, "Servo control of the position and size of an optical scanning system," *Proc. I.E.E.* (London), Part IV, vol. 101, pp. 129–134; February, 1954.
(68) "FOSDIC—A film optical sensing device for input to computers," *Tech. Bull. Nat. Bur. Stand.*, vol. 38, pp. 24–27; February, 1954.

Analog Techniques

A number of new analog techniques have appeared, particularly for the difficult problem of multiplication.

(69) M. Mehron and W. Otto, "Instantaneous multiplier for computers," *Electronics*, vol. 27, pp. 144–148; February, 1954.
(70) G. G. Savant, Jr., and R. C. Howard, "Multiplier for analog computer," *Electronics*, vol. 27, pp. 144–147; September, 1954.
(71) K. H. Norsworthy, "A simple electronic multiplier," *Electronic Eng.* (London), vol. 26, pp. 72–75; February, 1954.
(72) D. W. Slaughter, "Time-shared amplifier stabilizes computers," *Electronics*, vol. 27, pp. 188–190; April, 1954.
(73) M. A. Mayer, B. M. Gordon and R. N. Nicola, "An operational-digital feedback divider," *Trans. I.R.E.*, vol. EC-3, pp. 17–20; March, 1954.
(74) J. L. Douce, "A simple analogue divider," *Electronic Eng.* (London), vol. 26, pp. 155–156; April, 1954.
(75) H. Freeman and E. Parsons, "A time-sharing analog multiplier," *Trans. I.R.E.*, vol. EC-3, pp. 11–17; March, 1954.
(76) E. J. Angelo, "An electron-beam tube for analog multiplication," *Rev. Sci. Instr.*, vol. 25, pp. 280–284; March, 1954.

Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. All articles and books reviewed are numbered sequentially for each year; where known the Universal Decimal Classification number is also given. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.

H. D. Huskey, Editor

GENERAL

55-1

An Algebraic Theory for Use in Digital Computer Design—E. C. Nelson. (*Trans. I.R.E.*, vol. EC-3, pp. 12–21; September, 1954.) An algebraic theory of the logical operation of digital computers is developed. This theory takes into account the dynamic (time) behavior of computer processes. The computer signals and computer elements are described. Their properties, which are pertinent to the logical operation of digital computers, are abstracted and formulated in mathematical terms. The signals are represented by algebraic symbols, and the way they are transformed by the elements of the computer is represented in terms of algebraic operations and functions. This computer algebra is based on Boolean algebra. Time is treated as a discrete variable and a method of taking into account the time relationships in the computer process is developed. Specific components, such as gates, flip-flops, and magnetic drums, are analyzed, and an algebraic description of their operation is obtained.

Courtesy of Proc. I.R.E.

55-2

Application of Boolean Algebra to Switching Circuit Design and to Error Detection—D. E. Muller. (*Trans. I.R.E.*, vol. EC-3, pp. 6–12; September, 1954.) A solution is sought to the general problem of simplifying switching circuits that have more than one output. The mathematical treatment of the problem applies only to circuits that may be represented by "polynomials" in Boolean algebra. It is shown that certain parts of the multiple output problem for such circuits may be reduced to a single output problem whose inputs are equal in number to the sum of the numbers of inputs and outputs in the original problem. A particularly simple reduction may be effected in the case of two outputs. Various techniques are described for simplifying Boolean expressions, called "+polynomials," in which the operation "exclusive or" appears between terms. The methods described are particularly suitable for use with an automatic computer, and have been tested on the Illiac. An unexpected metric relationship is shown to exist between the members of certain classes of "+polynomials" called "nets." This relationship may be used for constructing error-detecting codes, provided the number of bits in the code is a power of two.

Courtesy of Proc. I.R.E.

55-3

Analytic Minimization I: Conjunctive Forms—W. C. Carter and A. S. Rettig. (*Jour. Computing Systems*, vol. 1, pp. 179–195; July, 1953.) This paper is devoted to showing that every Boolean formula can be put into a "Minimal" conjunctive form by the application of a few simple rules. "Minimal" here means that no conjunct or elements within a conjunct can be dropped without losing equivalence; not as is the more usual terminology, that the formula has the least number of symbols of any formula with which it is equivalent. The procedure involves transforming to a disjunctive form and then repeatedly using the laws $ABVAC=A(BVC)$, $ABVCD=(AVC)(AVD)(CVB)$ for $AC=0$ and $(A_1VA_2VA_3)(A_1VA_2VB=(A_1VA_2VA_3)\cdot(\bar{A}_3VB)$ for $A_1A_2A_3=0$. The resulting components can be further reduced, if necessary, by the application of test formulas. Rules for transformation and simplification are easy to apply. Errata: p. 180, ll. 11–12 should read: "$(C_1VC_2VC_3)$. (AVC_2VC_3). (BVC_2VC_3). (CVC_1VC_3). (DVC_1VC_2). (EVC_1VC_2)." p. 180, l. 18: "logical sum" is variously used in the literature. To remove ambiguity it should read either "conjunction" or "logical sum in the sense of Hilbert."

Norman M. Martin

55-4

Switching Functions on an n-Dimensional Cube—C. Y. Lee. (*Communication and Electronics*, no. 14, pp. 289–291; September, 1954.) A system is described for representing a switching function as a set of points on an n-dimensional cube. Through a study of the distances between the points it is claimed that the concept is of value in problems of discovering symmetries and of classifying types of switching functions.

R. K. Richards

55-5

A Digital Data-Recorder for Dense Storage of Continuous Voltages.—G. L. Hollander. (*Communication and Electronics*, no. 13, pp. 253–259; July, 1954.) A device is described for converting a voltage to a digital representation and recording the value on a 28-track magnetic tape. The precision of the data is plus or minus 0.5 per cent. The digital recording of nine separate information channels is provided; the sampling rate is 5,000 per second for one channel and 600 per second for each of the other eight. A block diagram of the system is presented and the principles of operation are explained. The physical volume of the system is an important consideration, and the volume required for 8 minutes of recording is 400 cubic inches.

R. K. Richards

55-6

A Digital Voltage Encoder—J. R. Zweizig. (*Trans. I.R.E.*, vol. EC-3, pp. 25–28; September, 1954.) A two-channel voltage encoder having a sampling rate of 40 numbers per second in each channel has been designed for use in a data reduction system. The data are recorded on single-channel magnetic tape in the form of 10-digit binary numbers with an accuracy of ± 0.1 per cent. The range of input voltage is 0 to 1 volt and may be lowered to 0 to 10 mv through the use of chopper amplifiers. This lower range of input voltage covers the voltages generated by analog transducers commonly employed to measure temperatures, pressures, flow rates, and thrusts.

Courtesy of Proc. I.R.E.

55-7

Precision High-Current Computer Power Supplies—A. B. Rosenstein. (*Communication and Electronics*, no. 14, pp. 405–409; September, 1954.) The requirements of power supplies for electronic computers are discussed in a general manner. The use of selenium rectifiers in combination with regulation by magnetic amplifiers for meeting these requirements is emphasized. The characteristics of the magnetic amplifier in this application are explained, and the important design considerations are presented for adapting this type of power supply system to computers.

R. K. Richards

ANALOG COMPONENT RESEARCH

55-8

Multiplier for Analog Computers—C. J. Savant, Jr., and R. C. Howard. (*Electronics*, vol. 27, pp. 144–147; September, 1954.) This article describes the theory and operation of the circuits used in an arbitrary function generator. The unit is essentially a multiplier. A two-input multiplier is described. Multiplication is obtained by taking the logarithm of the input signals, adding the logarithms and taking the antilog of the sum. The exponent of either signal may be changed by attenuating or amplifying the signal after taking the logarithm. All conversion from linear-to-log and log-to-linear is performed electronically. Sample problems and tests are described and results given. Obtainable accuracies are stated and possible methods

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—*The Editor*

of improvement are presented. The unit is flexible and can be used to determine rapidly nonlinear functions in feedback control systems design which give optimum response of the system.

Norman F. Loretz

55-9

A Function Generator for the Solution of Engineering Design Problems—C. J. Savant and R. C. Howard. (*Trans. I.R.E.*, vol. EC-3, pp. 34–38; September, 1954.) The solution of nonlinear engineering design problems demonstrates the need for a special function generator. The generator described in this paper satisfies this need. The basic components of the unit are discussed and the forms of functions which can be generated are shown. Accuracy is estimated by comparison of an oscillogram with the calculated curves. It is concluded from tests on the system that the function generator is a valuable aid in the handling of nonlinear design problems.

Courtesy of Proc. I.R.E

681.142 55-10

A Versatile Electronic Function Generator—R. Tomovich. (*Jour. Frank. Inst.*, vol. 257, pp. 109–120; February, 1954.) Two types of electronic circuit for performing any desired transformation on two arbitrary voltage waveforms are described. The general characteristics and accuracy of such devices when used in repetitive differential analyzers are discussed.

Courtesy of Proc. I.R.E. and *Wireless Engineer*

55-11

A New Method of Generating Functions—Lazarus G. Pelimerou. (*Trans. I.R.E.*, vol. EC-3, pp. 29–34; September, 1954.) As a result of a pressing need for function generators, a new method of function generation has been developed. The underlying principle of this function generator is the application of ordinary pulse techniques in such a way as to produce a function. The simplicity of design, the high accuracy attainable, the simple type of construction are the outstanding features of this general-purpose function generator. In order to compare this new type of function generator with those presently being used, three important types are discussed. These generators are of the general-purpose, electric and photoelectric types; other comparable electromechanical types are excluded.

Courtesy of Proc. I.R.E.

ANALOG EQUIPMENT

681.142:512 55-12

A Simplified Solution and New Application of an Analyser of Algebraic Polynomials—L. Lukaszewicz. (*Bull. Acad. Polon. Sci.*, vol. 1, pp. 103–107; 1953. In English.) A description is given of an analyzer circuit in which complex numbers are represented by sinusoidal voltages of frequency ~500 cps, with amplitude corresponding to the modulus and phase corresponding to the argument of the number.

Courtesy of Proc. I.R.E. and *Wireless Engineer*

UTILIZATION OF ANALOG EQUIPMENT

55-13

Rectifier Arc-Back Study on the Analogue Computer—J. K. Dillard and C. J. Baldwin, Jr. (*Communication and Electronics*, no. 13, pp. 198–208; July, 1954.) This paper is included because of the use of the word "computer" in the title. Actually, the device used in the study is more of a "miniature model" than a "computer."

R. K. Richards

Reliability of a Large REAC Installation—Bernard Loveman. (*Proc. Eastern Computer Conf., Joint IRE-AIEE-ACM, December 8–10, 1953, Washington, D. C.*, pp. 53–57; 1954.) Project cyclone (see *Proc. Western Comp. Conf.*, 1953, pp. 187–195. Review 53–61) contains 404 dc operational amplifiers of the chopper stabilized variety and supporting nonlinear equipment. The total tube count is about 3,000. It can be used in sections on four different problems or as a single system. It is argued that analog equipment of this type requires less reliability than equivalent digital equipment since solution time is less and many types of minor errors do not affect the solution appreciably. Error measuring means, suitable for calibration of precision resistors and potentiometers in summing amplifiers and mechanical servo multipliers, are given. Integrators are not mentioned. Most machine errors which may occur during computation are detected by a "true overload" indicator. This device continually examines the magnitude of the signal at the summing junction input grid of each amplifier and gives an alarm if this exceeds a few millivolts. Since errors are immediately indicated and localized and most equipment is plugged in, downtime is relatively small. During 1953, failure rates were 3.8 per cent per 1,000 hours for tubes, about an order of magnitude higher than equivalent digital computer experience. However, reliability was over 90 per cent since trouble location and repair are much easier.

William F. Gunning

DIGITAL COMPONENT RESEARCH

681.142 55-15

An Arithmetic Unit for Automatic Digital Computers—J. R. Stock. (*Z. angew. Math. und Phys.*, vol. 5, pp. 168–172; March 15, 1954. In English.) Discussion of the requirements for the arithmetic unit of a computer with magnetic-drum store, with particular reference to the computer for the Swiss Federal Institute of Technology. Operation with fixed or floating decimal point is provided for.

Courtesy of Proc. I.R.E. and *Wireless Engineer*

55-16

A Permanent High Speed Store for Use With Digital Computers—R. D. Ryan. (*Trans. I.R.E.*, vol. EC-3, pp. 2–5; September, 1954.) A new type of high-speed store is proposed for an electronic digital computer using interpretive program techniques. The store is based on the flying spot technique used in television signal generation. The information in the store may be read rapidly but is nonerasable. This store has the advantages of high storage density, good reliability and nonvolatility of information.

Courtesy of Proc. I.R.E.

55-17

An Improved Reading System for Magnetically Recorded Digital Data—Samuel Lubkin. (*Trans. I.R.E.*, vol. EC-3, pp. 22–25; September, 1954.) In magnetic recording of pulses, whether on drum or tape, the resulting flux pattern is affected by proximity of adjacent pulses. The best defined region is that adjacent to the maximum. In reading, the signal is the derivative of the flux. In the best defined region, this is close to a straight line passing through zero when the flux is maximum. The slope of the curve at the zero changes sign with change of pulse polarity. A new method of reading is described which examines the signal from the head for such transitions from positive to negative or reverse as indications that a positive or negative pulse had been recorded. This is done by gating the inverted signal with the delayed signal for positive pulse reading and the inverse of this for reading negative pulses. Besides providing sharply defined outputs, this method permits reading both positive and negative pulses from a single channel without interference or ambiguity. Examples are given for using this facility for checking purposes and for storage of two types of data in a common channel.

Courtesy of Proc. I.R.E.

55-18

Magnetic Drum Recording of Digital Data—A. S. Hoagland. (*Communication and Electronics*, no. 14, pp. 381–385; September, 1954.) Various factors to be considered in the design of a magnetic drum storage system are described. Major attention is devoted to the geometry of the system, and mathematical expressions are worked out to relate certain of the more important parameters.

R. K. Richards

55-19

Saturable Transformers as Gates—B. Moffat. (*Electronics*, vol. 27, pp. 174–176, 178; September, 1954.) In information-handling systems, saturable transformers and reactors can be used as gating devices as well as vacuum tubes and semiconductor diodes. This article describes, in general, the operation of both saturable transformers and reactors and describes in greater detail the design, construction, characteristics and use of the saturable transformer as a gating device. The saturable transformer described by the author is constructed of two ferrite cores and uses magnetic amplifier techniques in the winding arrangement so that the changes in the control current produce no signal at primary or secondary windings of the transformer. In order to test performance of the gate a four-input single-output channel selector was constructed. An output signal of 16 volts was obtained with an input pulse of 38 milliamperes amplitude and 2.5 microseconds width. Satisfactory operation was observed at a pulse repetition frequency of 150 kc.

Norman F. Loretz

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—*The Editor*

55-20

Notes on Decision Element Systems Using Various Practical Techniques—John D. Goodell. (*Jour. Computing Systems*, vol. 1, pp. 196–199; July, 1953.) The author illustrates the logic of decision elements by a system of magnetic decision elements and describes how the functions of decision, power gain, temporary storage, and pulse shaping are accomplished with such elements. He shows that any circuit of magnetic decision elements must be operated with a clock with two clock pulse trains. In the concluding portions of the article he discusses the effect on the problem of completeness of decision element sets of such a system. His statement (p. 197), "Under the conditions described, it is not possible to establish a complete system using only one type of element, for example, S," is unfortunately expressed. No circuit has been proposed for any element which is complete with the addition of a suitable delay element except *S*, and it is not, as the author illustrates, possible to construct a complete system with *S* (or *D*) alone. The results stated in the reviewer's "On Completeness of Decision Element Sets" (*Jour. Computing Systems*, vol. 1, no. 3, pp. 150–154) plus a few elementary considerations, yield the result that the minimal complete sets of decision elements for these conditions are sets 3–14 of the cited paper, and the sets containing *S* or *D* and one of the elements *A*, *B*, *E*, *G*, *K* or *R* (provided the clock pulse and no pulse can be used for information purposes). There are, consequently, 4 minimally complete sets with one and 20 with two elements (provided all elements have the same delay).

Norman N. Martin

55-21

Transistor Flip-Flop Uses Two Frequencies—R. L. Brock. (*Electronics*, vol. 27, pp. 175–177; June, 1954.) The flip-flop described is a new type of computer component. Essentially it is an oscillator capable of operating at either of two frequencies. The circuit is designed such that input pulses change the frequency of oscillation rather than a dc level as in conventional flip-flops. This circuit is adaptable to either transistors or electron tubes. However, the author states that many of the undesirable heating effects of on-off transistor flip-flop circuits are avoided because operation is closer to that of constant energy level. The rf output of the flip-flop may be passed through a suitable filter and then shaped into a pulse and used to trigger subsequent flip-flop stages. Various flip-flops of the type described have been built and tested. Successful operation was obtained from zero frequency to 5 kc, the highest repetition rate attempted. Schematics of tested flip-flops and a counter-coupling network are shown.

Norman F. Loretz

55-22

Quarterly Report No. 3, Second Series—J. R. Bowman, F. A. Schwertz, *et al.* (*Quart. Rept. Computer Components Fellowship Mellen Inst.*, 88 pp.; April 1, 1954 to June 30, 1954.) This report is divided into two main parts. The first part, comprising the first three sections, deals with electro-optical phenomena and electro-optical devices of potential importance in digital data-handling systems. The second part, comprising the last three sections, deals with printed circuitry and integral circuit construction techniques. In Section I a number of electro-optical devices are discussed, namely: (1) a bistable solid-state diode, (2) a bistable vacuum diode, (3) a solid-state image intensifier or amplifier and (4) various self-luminous displays. Sections II and III deal with ac and dc electroluminescent light sources respectively. Section IV contains some notes on insulating metal oxide films and Section V some data on transparent semiconducting metal oxide films. Section VI contains an account of some attempts to produce conducting metal lines or "printed circuits" by means of xerographic techniques.

F. A. Schwertz

55-23

Quarterly Report No. 4, Second Series—J. R. Bowman, F. A. Schwertz, *et al.* (*Quart. Rept. Computer Components Fellowship Mellen Inst.*, 92 pp.; July 1, 1954, to September 30, 1954.) Section I of this report contains an account of the first successful attempts to print conductive silver lines on glass substrates with the aid of xerographic techniques. Section II comprises a general discussion of xeroprinting, its advantages and range of application. Section III has to do with thin insulating films and methods of preparing same. A note on silicon monoxide capacitors is included. In Section IV data are presented on the temperature-dependence of the resistivity of thin transparent films of antimony-doped tin oxide formed on glass substrates. The frequency- and voltage-dependence of the average light output of ac electroluminescent light sources is discussed in Section V. Nine different electroluminescent phosphors were studied. It has been shown experimentally (*Quart. Progress Rept. No. 1, Second Series*, Review 54–146) that a vacuum diode comprising a photocathode and a phosphoranode may be switched from the conducting to the non-conducting state, and vice versa, by light pulses alone. A theoretical criterion for the stability of the conducting state has been developed and is discussed in Section VI.

F. A. Schwertz

DIGITAL SYSTEMS RESEARCH

55-24

Business Data Processing: A Case Study. Introduction—Richard G. Canning. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 80–81; April, 1954.) A study of inventory control in the ready-to-wear departments of a large department store was made especially for this conference. The proposed automatic data processing equipment was designed according to the "central records" or "delayed central processing" concept. Records accumulated in various departments are brought together in a control office for processing. Another possible point of view might have been the "specialized machine" approach in which small machines would be installed in each department, with integration of data to follow later. A third possible approach could have been the "real-time processing" method in which a special machine handles limited types of high activity transactions and a central machine handles the slower transactions.

E. P. Little

55-25

Business Data Processing: A Case Study. Ready-to-Wear Unit Control Procedure—S. J. Shaffer. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 82–88; April, 1954.) Present procedures were outlined for the handling of inventory and sales information for thirty-one ready-to-wear departments in four large department stores. The unit-control work is all performed in two centrally located offices. Procedures commence with the preparation and attachment of a price ticket as the merchandise is received, and conclude with the preparation of various daily, monthly and seasonal records and reports. The system identifies items by department, season, classification, manufacturers, style, color, size and price. Price changes, returned goods, cash or charge sales, and interstore transfers are recorded for about 20,000 transactions per day. Daily selling reports, monthly and six-monthly price-line sales records, and buyer's "Black Book" records are prepared by unit-control personnel, a group of about 25.

E. P. Little

55-26

Business Data Processing: A Case Study. Unit Control System Engineering—Raymond Davis. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 89–95; April, 1954.) People working on department store mechanization generally agree that sales data should be captured at the point of sale. A special point-of-sale recorder is proposed into which merchandise and clerk identification tags can be placed. Suitable information is printed on these tags and also recorded by magnetic ink, in binary coded decimal form. This information is transferred by contact recording to a magnetic tape and then condensed by transfer techniques to a high density (100 bits per inch). A similar tape is produced at the receiving department where the tags are prepared for the merchandise. This tape is processed with the master inventory tape in the morning to up-date it. The selling tapes are processed similarly at the end of the day, and the various reports prepared. Data for about 200,000 items are recorded on the master tape. No attempt is made to include methods of mechanizing the accounts receivable or accounts payable functions.

E. P. Little

55-27

Business Data Processing: A Case Study. A Solution for Automatic Unit Control—Harry D. Huskey. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 96–97; April, 1954.) Real case and ingenuity must be exercised in designing a computing system for a specific function, such as automatic unit control. Most of the digits handled by the system will be for identification only. Very little arithmetic work will be required. Special commands such as "read next item from sales activity tape, read next item from inventory tape, compare identifying portion

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of code, if these are in agreement then carry out certain mathematical processes, if not, then advance to next inventory position" should be developed. An "extraction-add" command to process a specific set of digits from a word and then return the new information to the same place in the word would be valuable. The author suggests other new commands, but warns against making the machine so specialized that it cannot be modified to handle changes in the inventory system of the store. A special recirculating code register using a "no address" type of operation is suggested.

E. P. Little

55-28

Business Data Processing: A Case Study. The System in Operation—Myron J. Mendelson. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 98–104; April, 1954.) The final burden of preparing a computer to process information in a data handling system falls on the programmer. He must reconcile the computer properties with the information requirements and suggest possible changes for an efficient and effective procedure. A flow diagram for a proposed unit-control system is given. Special activities tapes, transaction tapes and daily receiving tapes are sorted into master inventory tape sequence, then processed through the computer to give a new master tape, a new transaction tape and special reports on tab cards. The new transaction tape is then sorted into a sequence suitable for preparing the daily activities report. Sorting on tapes is slow, but present technology dictates that a moderately priced system suitable for processing 20,000 transactions daily for an inventory of 200,000 items must use tapes. The properties of tape handling units of a machine, therefore, assume tremendous importance for the efficiency of a data processing system.

E. P. Little

DIGITAL EQUIPMENT

55-29

A Survey of Automatic Digital Computers—U. S. Office of Naval Research. (Washington, vi+109 pp.; 1953.) This compendium of data on automatic digital computers incorporates the results of surveys by the Flight Research Laboratory, Wright-Patterson Air Force Base, and the Mathematical Sciences Division, Office of Naval Research. Included in the survey is one page of information on each of ninety-eight computers, among which are included machines in use, or under development, in Australia, Belgium, Canada, England, France, Germany, Holland, Japan, Norway, Sweden, Switzerland and the United States. A partial listing of the information given on the computers included in the survey is the builder, location of installations, availability of programming service and computing time, operating schedule, number base, word length, instruction type, sequence control, built-in operations and time required for their execution, description of internal storage and listing of input-output devices. The Office of Naval Research survey is a useful reference for workers in the automatic digital computer field and also for those who, though not concerned with their development, are interested in the application of high-speed digital computers.

E. W. Cannon

Courtesy of *Mathematical Tables and other Aids to Computation*

55-30

The MIT Magnetic-Core Memory—William N. Papian. (*Proc. Eastern Computer Conf., Joint IRE-AIEE-ACM, December 8–10, 1953, Washington, D. C.*, pp. 37–42; 1954.) A short review is first given of the coincident current mode of operation of a static, magnetic, parallel, binary, digital memory using square hysteresis loop nonmetallic ferromagnetic ferrite cores. Two banks, each storing $32\times32\times17$ bits on 90 mil O.D. cores, have been installed in the Whirlwind I Computer. Information is read out 2 microseconds after the request. 7 microseconds later (following red tape rewriting), a new address may be sampled in a completely independent memory access. Direct connected type 6080 tubes are used for 32X and 32Y read and write address drivers (128 altogether). Each delivers 450 ma within plus or minus 4 to 5 per cent. Seventeen "digit plane" drivers, similar to the address drivers, control the storing or rewriting cycle. Each reading signal (about 0.1 volt in amplitude for a "one"), feeds one of seventeen read amplifiers. The output is strobed 1.2 microseconds after the initiation of the address driver read pulse. Pictures and descriptions of core arrays and the installation with WW I are included. There are system block diagrams but no schematic diagrams. An investigation of sensitivity to variations of many operating parameters is described. WW I uses 16 bit words. The 17th bit in the memory is a parity check bit. This permits accurate error assignment. After only two months of operation, the memory chalked up a four-week error free period of over 460 hours, during which about 10^{11} memory consultations were made.

William F. Gunning

55-31

Testing Magnetic Decision Elements—J. D. Goodell. (*Electronics*, vol. 27, pp. 200, 202–203; January, 1954.) A short description of a test unit for magnetic decision elements is given in this article. Most of the article, however, describes the operation of the two basic elements. Schematics of the type *A* element (a mixer) and the type *S* element (a negative coincidence circuit) are shown. A photograph shows the standard size and subminiature size units. The magnetic elements consist only of inductors, diodes, and resistors. Input clock pulse power is derived from a pulse generator which provides two out-of-phase 100-kc strings of 5 microsecond pulses. Average power consumption per unit is approximately 0.5 watt.

Norman F. Loretz

55-32

The DIGITAC Airborne Control System—D. W. Burbeck, E. E. Bolles, W. E. Frady, and E. M. Grabbe. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 38–44; April, 1954.) This article describes the navigation system of which the Digitac is an airborne component, and sketches the historical steps in its development. It indicates some of the basic decisions that entered into the decision to make this airborne computer digital rather than analog. It also outlines briefly the mode of operation of the computer as the control element of the navigation system. The computer operates on information obtained from three ground stations consisting of pulse modulated transmitters. These stations operate in pairs, the difference in time of arrival of pulses at the aircraft from each pair establishes a line of position of the aircraft, the intersection of the two lines providing a fix. The airborne system measuring these time differences can provide an accuracy of one part in 30,000. The digital computer is required to calculate the position of the aircraft without loss of accuracy, and to provide appropriate steering signals to the aircraft. The fact that the measuring system output was in digital form leads to the initial consideration of a digital control computer. A study revealed that a general purpose computer has a flexibility and adaptability that might be exploited quite successfully—the development of a navigation system such as that described. The computer was tested on a C-47 aircraft and the delays caused by the time for making the required calculations produced no adverse dynamic effects. By the use of diode gating, and novel circuiting and logic, the computer was built with only 250 vacuum tubes. The computer uses an interesting method of solution, starting with the previously computed position and velocity data. All trigonometric calculations are effected using polynomial approximations, and square rooting is done using Newton's iterative technique. The computer is a serial binary machine using a magnetic drum memory, a 100 kc clock pulse rate, and words composed of 16 binary digits plus sign. The computer performs addition, subtraction, multiplication, division, check sign, as well as transfers to and from the input-output equipment. The magnetic drum has a storage capacity of 1,110 words, and one 6-word circulating register is provided for fast access storage. A floating address reference system is used to simplify the control equipment. At times the authors confuse the concepts of *precision* and *accuracy*, but this confusion is quite common. A reference to the "Report to the Association for Computing Machinery, First Glossary of Programming Terminology," published in June, 1954, by the Committee on Nomenclature, will be of help on this problem. In summary, the reviewer concurs in the following statement made in the article: "The Digitac System is an excellent example of a system's approach to a problem, in which the choice of a general purpose digital computer allowed the equipment design and construction to proceed even though the formulation of the system equations was not yet completed."

W. J. Schart

681.142 55-33

The System Design of the IBM Type 701 Computer—Werner Buchholz. (Proc. I.R.E., vol. 41, pp. 1262–1275; October, 1953.) This article records the basic philosophy and the design decisions which were made in connection with designing the IBM 701 computer. It describes the system in terms of logic without any reference to the ultimate physical equipment. The designers attempted to keep the amount of equipment

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to a minimum and avoid special-purpose equipment in order to increase reliability and decrease cost. The number system used in the 701 is binary with provisions for handling coded forms of decimal and alphabetic characters. The 701 has three types of high-speed storage: electrostatic, magnetic drum, and magnetic tape. The author explains the reasons for including all three and the purposes to which each is put. A table of instructions show the programming possibilities of the 701 computer. Other topics discussed include multiplication and division processes, shifting operations, overflow control, absolute-value representation, the rounding problem, the extract instruction, the "sense" instruction and a brief word on the absence of any large-scale built-in checking facilities. The 701 computer has an external system which includes card readers, card punches, printers, magnetic tape units and magnetic drum units. All of these units are controlled by the stored program. The copy and read instructions which permit words to be transferred between these units and the internal memory of the computer can handle, within wide limits, an arbitrary word length. The author discusses the advantages of this system, as well as the overlapping of input-output operations with internal operations. The starting procedure for the 701 includes a switch which determines whether the program is to be loaded from tape, cards, or drum. For longer programs the 701 works best with tape or drum programming, while cards make a convenient system for short programs. The new features claimed for the 701 computer include the following: (1) independently addressed half-words and full-words, (2) high-speed multiplication and division, (3) division with double-length dividends, (4) improved shift instructions, (5) flexible control of arithmetic overflow, (6) provision for manual alteration of a program predetermined by the internal program, (7) integration of all input-output equipment with the computer, (8) line-at-a-time printer capable of printing numeric or alphabetic characters, (9) variable record length for input, output, and external storage, (10) provision for flexible program control by tape or cards, and (11) programs substituting for equipment whenever possible, to achieve greater flexibility and reliability.

J. D. Chapline

UTILIZATION OF DIGITAL EQUIPMENT

55-34

Acceptance Test for Raytheon Hurricane Computer—F. J. Murray. (*Proc. Eastern Computer Conf., Joint IRE-AIEE-ACM, December 8–10, 1953, Washington, D. C.*, pp. 48–52; 1954.) This article is about equally divided between a description of the acceptance test used and of the Hurricane Computer itself. Because the Hurricane Computer was built on contract and was the first of its kind, very complete testing was required. Phase I of the main test demonstrated the abilities of the machine; Phase II was a demonstration of ability to process a large amount of information, and Phase III was the solution of a large system of differential equations. A number of special checks were performed on peripheral equipment and on the operation of the self-checking features. No information is given on time required for passage, number of attempts, and the like. Each section is extremely compact and covers in a remarkably complete manner a very extensive subject.

Sibyl M. Rock

55-35

SEAC—Review of Three Years of Operation—P. D. Shupe, Jr. and R. A. Kirsch. (*Proc. Eastern Computer Conf., Joint IRE-AIEE-ACM, December 8–10, 1953, Washington, D. C.*, pp. 83–90; 1954.) SEAC, originally conceived as an interim computing facility for government use, proved quite reliable and was therefore expanded and kept as a permanent facility at the National Bureau of Standards. Since it was an experimental machine, however, more time has been allotted to modification and development than would normally have been the case. Experimentation caused some loss of reliability at first, but has since served to improve the system. In this paper the authors describe operating and maintenance procedures and trouble-shooting techniques, and discuss the operating efficiency of the computer for the three-year period. A detailed analysis is given of machine failures for one particular month. Reliability data are given for vacuum tubes (6AN5's), germanium diodes, resistors, electromagnetic delay lines, and pulse transformers.

R. Lipkis

BOOK REVIEWS

55-36

Proceedings of Conference on Automatic Computing Machines, University of Sidney, Australia, August, 1951—(Melbourne, Commonwealth Scientific and Industrial Research Organization in conjunction with Electrical Engineering Dept. of Univ. of Sydney, 220 pp.; 1952.) The first of two sessions contained "An introduction to automatic calculating machines" and a paper entitled "Automatic digital calculating machines," both by D. R. Hartree. Two other papers discussed the C.S.I.R.O. (Commonwealth Scientific and Industrial Research Organization) Differential Analyser and the C.S.I.R.O. Radiophysics MK. 1 Automatic Computer. The latter is an acoustic-delay-line-memory digital computer with magnetic drum and punched card input-output. In the discussion of the use of superfluous binary digits for error-detecting which followed, Hartree considered that "the use of error detecting procedures at each operation of the machine was a counsel of despair." He felt that experience has shown that computers do not go wrong often enough to warrant this. In the second session, Hartree gave an introduction to programming using the EDSAC for illustration; he also presented a paper on numerical methods used with automatic calculating machines. The latter included a summary of various methods of determining roots of polynomial equations with automatic machines. T. Pearcey presented papers on programming for the C.S.I.R.O. digital machine and for punched-card machines, and on the functional design of an automatic computer. Some of the other papers presented were: (1) "Some analogue computing devices," (2) "Digital-analogue conversions," (3) "An analogue computer to solve polynomial equations with real coefficients," and (4) "Some new developments in equipment for high-speed digital machines." The last paper dealt with a high-speed magnetic switching device, a single electron tube scale-of-ten numerical displaying counter, a single tube which combines the functional operations of a bi-stable element and gate, giving several applications and details of a magnetic-drum digital storage system.

J. H. Wegstein

Courtesy of *Mathematical Tables and Other Aids to Computation.*

55-37

Probleme der Entwicklung programmgesteuerter Rechengeräte und Integrieranlagen—H. Bückner, F. J. Weyl, L. Biermann and K. Zuse. (Rhein.-Westf. Technische Hochschule Aachen, Mathematisches Institut, H. Cremer, ed., Aachen, xiii+75 pp.; 1953.) This book contains the essential contents of four speeches given at a colloquium in Aachen in July, 1952, under the sponsorship of the Institute for Mathematics, Mechanics, Physics and Theoretical Physics of the Rheinisch-Westfälischen Technischen Hochschule. The four chapters of the book, based upon the speeches of the authors in the order above, are the following: "Über die Entwicklung des Integremat"; "Aufbauprinzip, Arbeitsweise und Leistungsfähigkeit elektronischer programmgesteuerter Rechenautomaten und ihre Bedeutung für die naturwissenschaftliche Forschung"; "Die Gottinger Entwicklungen elektronischer Rechenautomaten"; "Über programmgesteuerte Rechengeräte für industrielle Verwendung." In the first chapter, Bückner gives a functional description of the Integremat, a differential analyzer. In the second chapter, by F. J. Weyl, the characteristics of electronic digital computers now in use in the United States are compared and some of their uses are discussed. Included in the comparison of machines is the primary motivation of their construction—ballistics computations, the development of improved components and more flexible computational systems, or commercial and industrial applications. In the third chapter, L. Biermann discusses the features of a new digital computer in operation at the Max Planck Institute of Physics. The computer is a moderate-speed, tape-fed, magnetic drum machine, operating on 32 binary-digit numbers, with a 3 binary-digit integral part. Some of the problems being solved on the computer are described. The last chapter, by Zuse, is an exposition of his development of relay computers, prefaced by a review of the difficulties he encountered up to the time of the installation of a Zuse computer in the Eidgenössische Technische Hochschule at Zürich in 1950. He presents an interesting explanation of the reasoning underlying many of his design decisions, and states a case for moderate speed, simple-to-operate computers, particularly for application to engineering problems. The book closes with a recording of the discussion which ensued after the presentation of the papers.

E. W. Cannon

Courtesy of *Mathematical Tables and other Aids to Computation*

EDITOR'S NOTE: In the December, 1954, issue, acknowledgment to *The Scientific Monthly* for Review **54-213** was inadvertently omitted.

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—The Editor

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